

What's New in Version 16.9.69 Service Release 2

BOM AND CENTROIDS

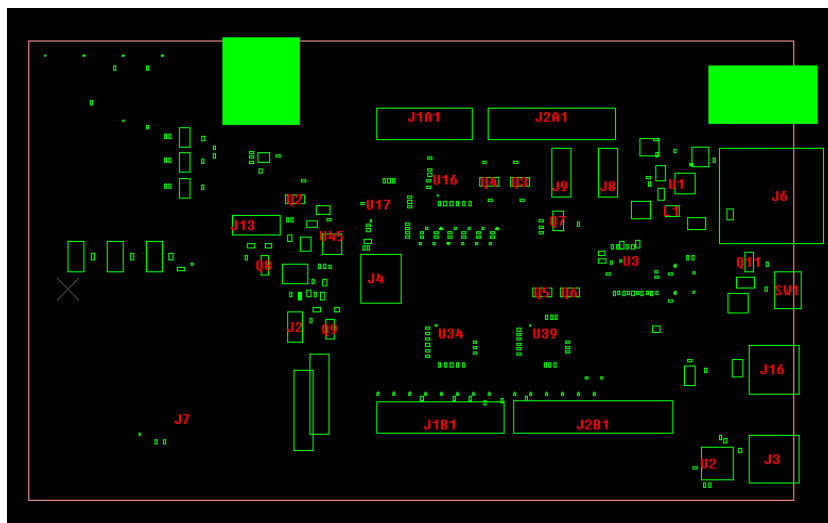
- NEW - Enhancements in VisualCAM's BOM report now allow you to easily create Centroid files in any order including an option to mirror the backside when exporting the Centroid file.

You now have the ability to change the "Populate" settings in your BOMs indicating whether or not to insert (populate) each component during placement. You are able to do this paperless by using the "Populate" function in 2581. You can now see what is included in the BOM and which parts are to be inserted and which parts are not. This is extremely valuable during PCB Assembly setup and at the placement machine to review your data on screen in real time.

Set a components populate attribute value or compare BOM's of different assemblies and update the BOM automatically to reset the Populate setting in the file. You can now view this data in the BOM and graphically display on screen using VisualCAM.

Ref Des	Device	Footprint	Side	Pin 1 Loc	# of Pins	Angle	Part Number	Centroid Loc	Ref Des Loc	Insertion Loc	Value	Tolerance	Description	Populate
C1	SMC...	SMCO602...	Top	3.73260...	2	180.0	602433-081	3.732602:0...	3.732602...	3.732602:0...	22UF		602433-081	true
C3	C020...	C0201	Top	3.82083...	2	0.0	C83410-027	3.820835:0...	3.820835...	3.820835:0...	0.1uF		CAP_C02...	false
C4	SMC...	SMCO201	Top	3.91189...	2	0.0	C83410-017	3.922398:0...	3.922398...	3.922398:0...	330...		C83410-0...	false
C5	SMC...	SMCO402	Top	1.45863...	2	0.0	A36096-114	1.458630:0...	1.458630...	1.458630:0...	10uF	20%	G21049-0...	false
C6	C020...	C0201	Top	1.55491...	2	180.0	C83410-014	1.554913:0...	1.554913...	1.554913:0...	0.1uF		CAP_C02...	true
C8	SMC...	SMCO402	Top	1.51608...	2	0.0	A36096-114	1.516087:0...	1.516087...	1.516087:0...	10uF	20%	G21049-0...	true
C9	C020...	C0201	Top	4.10583...	2	0.0	C83410-014	4.105835:0...	4.105835...	4.105835:0...	0.1uF		CAP_C02...	true
C10	C020...	C0201	Top	4.00740...	2	180.0	C83410-014	4.007409:1...	4.007409...	4.007409:1...	0.1uF		CAP_C02...	true
C11	SMC...	SMCO402	Top	3.37792...	2	270.0	A36096-114	3.360421:0...	3.360421...	3.360421:0...	10uF	20%	G21049-0...	true
C12	C020...	C0201	Top	3.41729...	2	180.0	C83410-014	3.417291:0...	3.417291...	3.417291:0...	0.1uF		CAP_C02...	true
C13	SMC...	SMCO402	Top	3.58461...	2	180.0	A36096-114	3.584614:0...	3.584614...	3.584614:0...	10uF	20%	G21049-0...	true
C14	C020...	C0201	Top	3.55508...	2	0.0	C83410-014	3.555087:0...	3.555087...	3.555087:0...	0.1uF		CAP_C02...	true
C15	C020...	C0201	Top	2.65941...	2	90.0	C83410-014	2.669917:0...	2.669917...	2.669917:0...	0.1uF		CAP_C02...	true
C16	C020...	C0201	Top	2.57083...	2	90.0	C83410-014	2.581335:0...	2.581335...	2.581335:0...	0.1uF		CAP_C02...	true
C17	C020...	C0201	Top	2.48225...	2	90.0	C83410-014	2.492752:0...	2.492752...	2.492752:0...	0.1uF		CAP_C02...	true
C18	C020...	C0201	Top	2.39366...	2	90.0	C83410-014	2.404169:0...	2.404169...	2.404169:0...	0.1uF		CAP_C02...	true
C19	C020...	C0201	Top	2.30508...	2	90.0	C83410-014	2.315587:0...	2.315587...	2.315587:0...	0.1uF		CAP_C02...	true
C20	C020...	C0201	Top	2.21650...	2	90.0	C83410-014	2.227004:0...	2.227004...	2.227004:0...	0.1uF		CAP_C02...	true

View and Sort Components in the BOM including the populate status and get the centroid data needed for Assembly.



View the Assembly Outlines as described in the 2581 file on screen, the filled areas are making use of the "Populate" element in IPC-2581 to show the parts that are not to be installed for ease of verification during Assembly.

Fabrication Reports

Pushing for paperless, you can now visualize the information needed to manufacture your design by using the new Fabrication Reports. Take a quick look inside at the stackup with a graphic depiction including the Impedance, Board information, Designer Notes, Standard Notes, Drill Spans. Also included in the report are Dimension Drawing, Hole Chart, and Assembly Top and Bottom. This new report allows further access to the information inside your IPC2581 file.

Fabrication Report

Design Name: Edison_arduino-IPC2581-Demo-Full_2581B
 Panel Number:
 Total Layers: 4

VisualCAM 16.9
 June 18, 2018
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Layer	Thickness	Function	Material	Impedance	Df	Dk	Drill Span
SILKSCREEN_TOP	0.000394	SILKSCREEN	EPOXY_INK_UV_CURE				
ENIG_TOP	0.000181	COATINGCOND	ENIG				
SOLDERMASK_TOP	0.000472	SOLDERMASK	SOLDERMASK_FLEXIBLE_UV_CURE				
TOP	0.001902	CONDUCTOR	COPPER	Yes			
DIELECTRIC_INDEX_5	0.004000	DIELPREG	370HR		4.5	0.0211	
GND	0.001299	PLANE	COPPER				
DIELECTRIC_INDEX_7	0.004000	DIELPREG	370HR		4.5	0.0211	
PWR_GND	0.001299	PLANE	COPPER				
DIELECTRIC_INDEX_9	0.004000	DIELPREG	370HR		4.5	0.0211	
BOTTOM	0.001902	CONDUCTOR	COPPER	Yes			
SOLDERMASK_BOTTOM	0.000472	SOLDERMASK	SOLDERMASK_FLEXIBLE_UV_CURE				
ENIG_BOTTOM	0.000181	COATINGCOND	ENIG				
SILKSCREEN_BOTTOM	0.000394	SILKSCREEN	EPOXY_INK_UV_CURE				

Designer Notes:

Design Name: Edison_arduino-IPC2581-Demo-Full_2581B

- All line neck downs and changes to differential line width and space are of design intent.
- Use artwork FILLED_VIA for holes that are to be filled with Peters 2795 or equivalent non-conductive resin. These are the plated COH Chip on hole or pad on via type vias to be plated over on both sides.
- The filled and plated over via is considered the most complex feature. The Fujitsu daisy chain coupon must contain the filled via feature.
- Tent vias on top layer using artwork TENT_VIA_TOP. Tent vias on bottom using artwork TENT_VIA_BOTTOM.
- Breakout from the center of any Non-Plated Through Hole into other nearby Non-Plated Through Hole is not acceptable, some material must remain between holes. Less than 6 mils or 0.52 mm minimum clearance between Non-Plated Through Holes is permitted on this design.

Standard Notes - INSTRUCTION:

Design Name: Edison_arduino-IPC2581-Demo-Full_2581B

- DF Standard 900/014 is the purchase specification that lists many of the requirements for this design. The specification also lists acceptable deviations that may be applied if necessary. The specification labeled DESIGNER_NOTES will take precedence when conflicting information between DF Standard 900/014 or other FNC specifications occur
- It is acceptable to change the MADE IN USA text on the silkscreen layer to that of the actual country where the board is fabricated.
- The PanelProfile layer contains the rout data
- The V-Score layer contains the v-score data.

Board Information:

Design Name: Edison_arduino-IPC2581-Demo-Full_2581B

Units: Inches
 Board Thickness: 0.020496063
 Minimum Trace Width: 0.00 (+/- 10.00%)
 Minimum Trace Spacing: 0.00 (+/- 10.00%)
 Surface Finish: HASL

Compliance Notes - OTHER:

Design Name: Edison_arduino-IPC2581-Demo-Full_2581B

- 1 UL Standard
- 2 Telcordia GR-78-Core

Controlled Impedance Required:

Design Name: Edison_arduino-IPC2581-Demo-Full_2581B

Layer: TOP CONDUCTOR COPPER Thickness: 0.001902

- | | |
|---|--|
| <ol style="list-style-type: none"> 1. EDGE_COUPLED
MICROSTRIP_MASK_COVERED
Ohms: 90
Trace Width: 90
Differential Pair Spacing: 0.127
Co-Planar Spacing: 0.00
Reference Plane: L8:GND | <ol style="list-style-type: none"> 2. SINGLE_ENDED
MICROSTRIP_MASK_COVERED
Ohms: 50
Trace Width: 50
Differential Pair Spacing: 0.00
Co-Planar Spacing: 0.00
Reference Plane: L8:GND |
|---|--|

Layer: BOTTOM CONDUCTOR COPPER Thickness: 0.001902

- | | |
|---|--|
| <ol style="list-style-type: none"> 1. EDGE_COUPLED
MICROSTRIP_MASK_COVERED
Ohms: 90
Trace Width: 90
Differential Pair Spacing: 0.127
Co-Planar Spacing: 0.00
Reference Plane: L8:PWR_GND | <ol style="list-style-type: none"> 2. SINGLE_ENDED
MICROSTRIP_MASK_COVERED
Ohms: 50
Trace Width: 50
Differential Pair Spacing: 0.00
Co-Planar Spacing: 0.00
Reference Plane: L8:PWR_GND |
|---|--|

NEW IN STACKUP

- 11612 WSSI_SITE now supports a Company Logo in the Stackup Report
- 11600 Stackup Report now supports nsaProfileDrawing name
- 11438 Stackup Editor - Added Dielectric Constant (Df), Loss Tangent (Dk) and Drill Span columns. You can now select columns to be turned off.
- 11485 Added support to WSSI_SITE for Stackup Report .ini file settings
- 11439 NEW Feature - Fabrication Report added to the Stackup Editor- Include Stackup, Impedance, Drill Span, Notes, Hole Chart, Dimensions, Assembly Component Layer and more...

FIXED IN STACKUP

- 11564 Stackup Report - Controlled Impedance - Trace Width value is wrong
- 11560 Stackup Notes - Multi Line issue when data is cut and pasted into the Notes editor
- 11559 Stackup Editor - Board Thickness setting dialog opens when dialog is opening
- 11545 Stackup Units - Board Info - Need to remove the possible confusion of having two units in the same database
- 11553 LoadStackup macro command not loading file saved from SaveStackup macro command
- 11535 Units behave strangely in Board Info section of Stackup Editor

PANELIZE

- 11579 FIXED - Simple Panelize without virtualization is not working in the latest build
- 11565 FIXED - Virtual Panel - Multiple panels not regenerating correctly
- 11547 FIXED - Virtual Panel not working properly when editing the virtual panel layer set afterward

DRC/DFM

- 11557 NEW - Print Errors in Color and show both layers overlaid for Layer Compare errors
- 11568 NEW - "Print All" DRC/DFM Error Reports now print to one PDF file with Multiple pages
- 11563 FIXED - Isolated Pad Removal on Buried Layers
- 11576 FIXED - Via to Pin not finding these errors
- 11542 FIXED - Window mode always set in analysis of design file once set

NC

- 11607 FIXED - Import of NC Slot issue
- 11518 FIXED - Drill chart ignores rotation / SR 600038035

ODB++

- 11594 FIXED - These ODB++ designs from Valor don't import due to unrecognized data
- 11582 FIXED - FPL merge in ODB++ Library
- 11582 FIXED - Problem with merge in ODB++ based FPL

IPC-2581

- 11546 NEW - Add Prompt the User on Export of IPC-2581 if the Dimension Units don't match the Database
- 11590 FIXED - Issue loading in Zuken IPC2581 file
- 11473 FIXED - Missing pads after export 2581 and then re-import

GERBER

- 11539 FIXED - Gerber import issue with extremely fine features

GENCAD

- 11448 FIXED - Gencad Import - outline/centroid issue

MACROS

- 11664 FIXED - AddPanelHoleChart Macro that failed to add hole chart on this design
- 11643 NEW - AddPanelFiducialSet adds Mask, Top and Bottom Shape and Size to use
- 11596 NEW - User ID (UID 1010) Macro to assist in creation of custom drill to mask report
- 11575 FIXED - Pad Removal Macro Command should not run on PhyNet Layer
- 11570 NEW - User ID (UID 1008 and UID 1009) Macro to convert draws, arcs, polylines to individual drill hits on a new NC layer, with user specified pitch and number of revolutions.
- 11566 NEW - GetFirstItem optional argument to use the select filter
- 11556 NEW - LogMessage Macro to write messages to the log
- 11522 NEW - Add IsEmptyLayer, IsFreeLayer, and GetLayerFromType macro commands
- 11500 NEW - Macro command to SetLayerOrder
- 11499 FIXED - ADDVIEWTAB macro window values are MM instead of Inch
- 11492 NEW - Macro command to combine apertures of the same size
- 11490 FIXED - Stacked Pad Removal Macro command to honor Layer parameter
- 11452 NEW - Macro command to add Dimensions - Linear and Ordinate
- 11451 FIXED - Create Panel from IDF Macro command needs to remove duplicate drills
- 11449 NEW - "SetAsVia" macro command added to set "Gerber" pads as via for use with DFM checks
- 4205 NEW - Allows you to clip all data inside or outside the border on a layer

FIXED MISC

- 11641 Convert Drawn Pads problem with asymmetrical shape replacement
- 11629 D0 errors after running Teardrop command
- 11427 Overlay mode red background issue
- 11506 Ghost apertures left behind after layer deletion
- 11482 Compact Aperture List issue
- 11501 Fixed loading in v15.GTD files that had duplicate unique id's

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- 11433 Fixed an issue with Automatic Draw Conversion
- 11430 ARE - When doing 2 pin ambiguity check - order the candidate parts
- 11428 Addlayer Parameter of LOADSTACKUP macro should become its own separate command
- 11420 Add pin #1 marker to createsilkscreen macro
- 11415 Rotated Pad - Paste issue
- 11425 Fixed issued with LOADSTACKUP macro command

Version 16.9 (16.9.42)

Initial Release of VisualCAM 16.9 (64-bit)

