Cadence Sigrity SystemSI Signal Integrity Solutions

Accurately assess high-speed, chip-to-chip system designs

Cadence® Sigrity™ SystemSI™ signal integrity (SI) solutions provide a comprehensive and flexible SI analysis environment for accurately assessing high-speed, chip-to-chip system designs. A block-based editor makes it easy to get started. The solutions support industry-standard model formats and automatically connect the models. With a unique combination of frequency domain, time domain, and statistical analysis techniques, you can be confident of achieving robust parallel bus and serial link interface implementations.

Benefits

Use SystemSI to:

- Perform detailed SI analysis of high-speed parallel buses and serial links
- Perform die-to-die analysis pre-layout, post-layout, or anywhere in between
- Verify interfaces will be compliant with interface performance standards
- Concurrently evaluate SI effects such as losses, reflections, crosstalk, and simultaneous switching output (SSO)
- Observe the impact of non-ideal power delivery system effects on system behavior
- Improve design quality by identifying potential SSO problems in parallel buses
- Develop, test, and utilize IBIS AMI TX and RX models for serial link analysis
- Quantify the bit error rate (BER) and performance of complex SerDes channels
- Reduce costs and time by identifying potential problems early

Features

SystemSI Parallel Bus Analysis approach

Today's high-speed bus interfaces, such as DDRx memory designs, are characterized by tight timing margins and analysis requirements that cross chip, package, and board structures. With the SystemSI Parallel Bus Analysis approach, you get support for concurrent simulation that accounts for the effects of dielectric and conductor losses, reflections, inter-symbol interference (ISI), crosstalk, and simultaneous switching noise (SSN). This is essential for emulating real hardware behavior.

SystemSI Serial Link Analysis approach

Assuring robust operation of high-speed serial links is challenging as data rates climb into the multi-gigabit

Figure 1: Simulation results for a DDR3 interface including a memory controller and SDRAM

realm. The SystemSI Serial Link Analysis approach simulates end-to-end channel behavior to produce comprehensive eye diagrams and bathtub curves and to predict BER performance.

By identifying jitter and noise impacts, you can quickly make design improvements. The tool fully supports industry-standard IBIS AMI TX and RX models in simulations that assess the effectiveness of chip-level signal conditioning along with clock and data recovery.

Enhanced design flow

SystemSI includes an easily used block-based topology editor to rapidly capture a single net or a complete multi-board bus. With a wizard and basic templates, you can start your design process early, and swap in progressively refined models as your design takes shape.

To maximize accuracy, you can use detailed S-parameter models, generated from tools such as Cadence Sigrity PowerSI® technology. The Cadence open Model Connection Protocol (MCP) simplifies and automates the hook-up, so you can avoid tedious and error-prone model connection tasks. Compliance kits and graphic- and text-based outputs help you quickly identify potential risks.

Maximum accuracy

Assuming an ideal power delivery network (PDN) is extremely dangerous for high-speed designs. Noise is easily propagated in boards and packages due to the low-loss nature of the substrate materials used. In designs that approach multi-gigabit operating speeds, eye quality can be significantly impacted by the presence of even small noise currents in the PDN.

Sigrity tools extract signals coupled with the associated PDN, enabling simulations that account for these real-time interactions. This is essential because the impact of PDN noise can rival and even surpass traditional signal-to-noise crosstalk. The ability to utilize structurally correct SPICE subcircuits for the I/O circuit models enables SystemSI to include these effects that are typically masked in other tools.

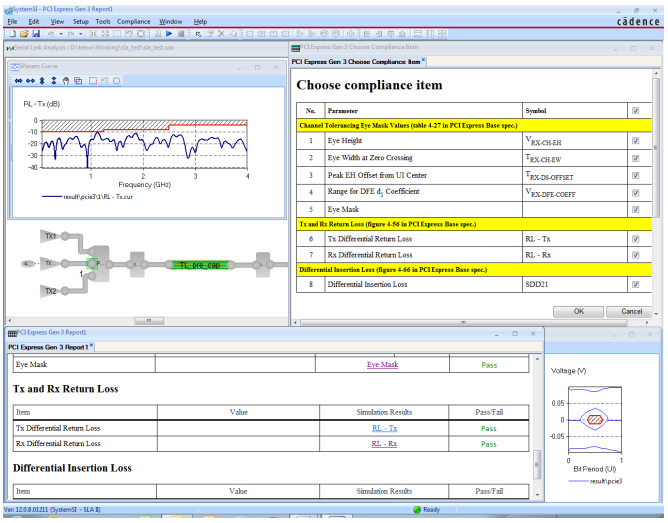

Figure2: PCI Express Gen3 SerDes simulation incorporating IBIS AMI models and accounting for back-channel simulations

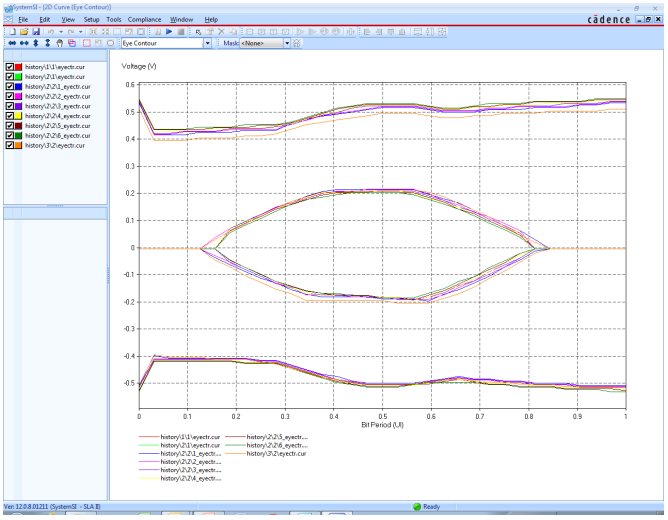

Figure 3: Eye contours showing the impacts of power noise

Supported Interfaces

- Available for use with Windows and Linux
- Models: SPICE (HSPICE and others), IBIS (native IBIS, BIRD95/98, AMI), S-parameters (Touchstone/Cadence Sigrity Broadband Network Parameter (BNP) syntax), Cadence Sigrity MCP
- Parallel bus interface compliance checks included for DDR2, DDR3, LPDDR3, DDR4
- Serial Link compliance checks included for PCIe 3.0, SFP+, 10G Base KR, HDMI, USB 3.0

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