cadence®

Cadence PCB Signal and Power Integrity

Streamlining the creation of high-speed interconnect on digital PCBs

The Cadence® integrated high-speed design and analysis environment streamlines creation of high-speed interconnect on digital PCBs. A range of capabilities—from simple to advanced—enable electrical engineers to explore, optimize, and resolve issues related to signal integrity and power integrity at all stages of the design cycle. By enabling a constraint-driven design flow, this unique environment accelerates the time to first-pass design success while reducing the overall cost of end products.

Cadence PCB Signal and Power Integrity

Cadence PCB signal integrity (SI) and power integrity (PI) technologies provide a scalable, cost-effective pre- and post- layout system interconnect design and analysis environment. They deliver advanced analysis at the board and system levels. Cadence PCB SI and PI products integrate tightly with Cadence Allegro® PCB Designer and Allegro Design Authoring enabling end-to-end, constraint-driven, high-speed PCB system design.

Cadence PCB SI technology addresses the design challenges presented by increasing design density, faster data throughput, and shrinking product design schedules by enabling designers to deal with high-speed issues throughout the design process. This approach allows design teams to eliminate time-consuming iterations at the back-end of a design process. It also lets them maximize electrical performance while minimizing cost of the overall product. The IBIS modeling standard is supported natively in addition to Cadence DML support.

A transistor-level model import wizard prepares models to run with the native SPICE simulators. In addition, topology exploration with models representing manufacturing tolerances allows engineers to improve production yields.

Cadence PCB SI technology eliminates the need to translate design databases to run simulations by providing a highly integrated design and analysis environment. Designers can also accurately address shrinking timing budgets by considering the effects of package design on the overall performance of the signal from die to die. The integrated flow is of great value to the designers, who now can easily perform pre- and post-layout extraction and verification of complex high-speed PCB systems.

Benefits

- Highly integrated design and analysis environment removes the need for error-prone and time-consuming design translation
- Intuitive pre-route analysis tools enable a design methodology that streamlines post-route design verification through a consistent front-to-back constraint management system
- Power stability and delivery are optimized through DC and AC power analysis
- Serial link design methodology supports pre- and post-route techniques that guide physical implementation, screen routed designs, and guide designers to the appropriate signals to perform fast, accurate, and detailed million-bit simulations using the latest industry-standard IBIS-AMI SerDes models
- Timing budgets of complex source-synchronous parallel interfaces can be efficiently validated with an optimized bus analysis solution

Features

Integrated High-Speed Design and Analysis

To eliminate the risk of design translation issues, Allegro PCB SI is seamlessly integrated with the Allegro PCB Designer and allows for constraints and models to be embedded in the board design file (see Figure 1). The integrated design and analysis system is aware of multi-net electrical constructs from logical design authoring to physical implementation. For

example, differential pairs and extended nets (nets with a series termination) are recognized, extracted, and simulated as one electrical net from either schematic or layout. The SigXplorer module integrates with logical or physical design tools and provides a graphical view of I/O buffers, transmission lines, and vias such that complex topologies can be modified in a what-if fashion—without having to change the actual design. SigXplorer also allows engineers to sweep various parameters within the topology to identify a topology solution space, which can then be captured in the constraint management system and guide PCB designers to first-pass electrical compliance. I/O buffers can be modeled using many popular techniques including industry standard IBIS models and encrypted SPICE models.

Constraint-Driven Design Methodology

Cadence PCB SI technology works seamlessly with the constraint management system. Constraints derived through simulation can be put into an electrical constraint set (EC set) from within the topology canvas, SigXplorer. These EC sets can then be applied to other nets in the design through the constraint management system found in Allegro PCB SI. Designers can use the constraints developed through simulation and exploration and enable a front- to back-end constraint-driven design process. (see Figure 2).

Power Integrity

Allegro PCB SI features both DC and AC power integrity capabilities. Allegro PCB SI includes static IR drop (DC) analysis technology that verifies that the power distribution system can provide sufficient current to drive signals. The analysis considers effects due to trace neckdown; Swiss-cheese planes created by components with dense pin grid arrays; and reduction of available copper caused by trace routing on power and ground planes. The analysis also takes into account all vias that connect multiple ground planes of the same net. Results can be viewed in a graphical voltage drop display (see Figure 3) or in a report that shows voltage drop at any pin that is

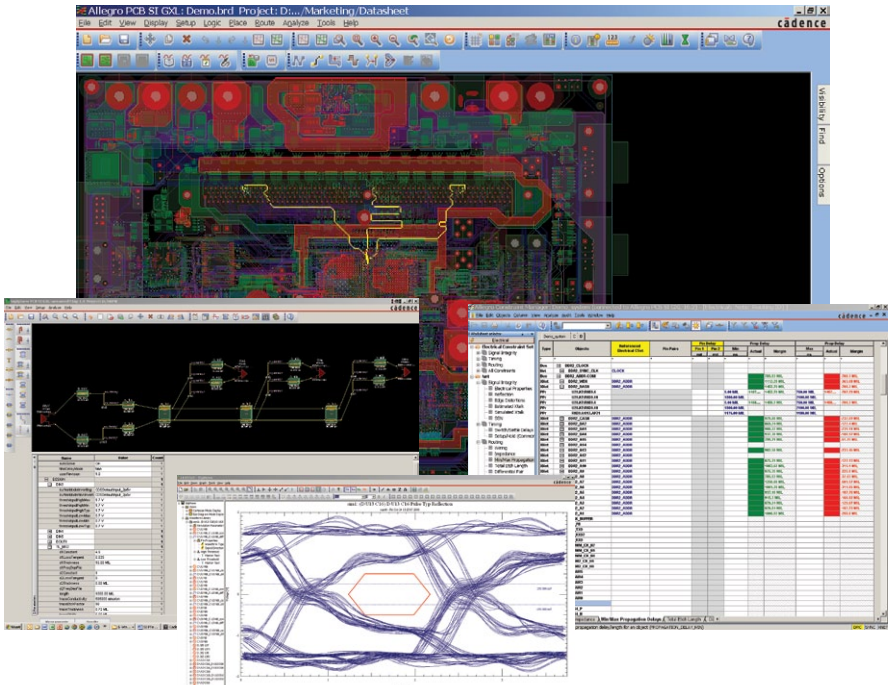

Figure 1: No translation is required to analyze selected signals from the physical board or extract them into the SigXplorer module; analysis results are reported in the same constraint manager used by Allegro PCB Designer

marked as a current sink. Users can also view relative and absolute voltage drop at any point on the net.

AC power integrity is accomplished with Allegro PCB PDN Analysis, an option to Allegro PCB SI. Its unique, integrated design and analysis environment takes the guesswork out of quantifying and controlling noise in power delivery systems. Engineers can focus on the design instead of struggling with data translation issues between the CAD system and the analysis engines. Allegro PCB PDN Analysis integrates proven technology into the Cadence design and analysis environment to address the power delivery issues encountered in high-speed design.

Frequency domain simulation allows users to quantify the impedance of the power delivery system across the frequency range of interest. In addition, the effectiveness of the decoupling capacitor selection and placement can be verified in the time domain, where ripples in the voltages can be measured and optimized.

Chip current profiles accurately characterize a target impedance in Allegro PCB PDN Analysis. In addition, capacitance on the chip and inductance from

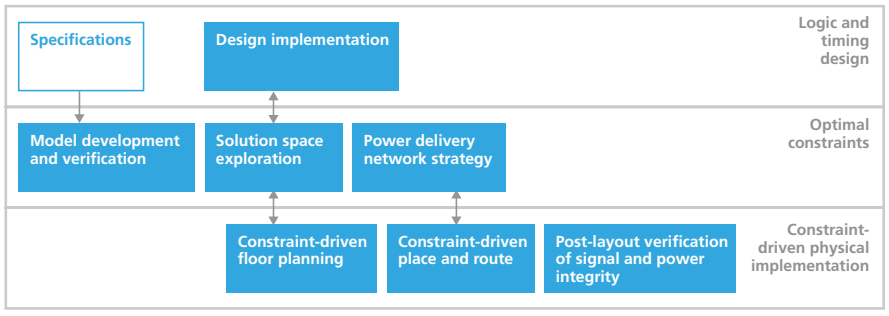

Figure 2: Allegro PCB SI and PCB PDN Analysis Option allows engineers to explore and develop optimum constraints and power decoupling strategies within a constraint-driven design flow

the package, or package and die power delivery models, can be assigned to an arbitrary position on a two-dimensional plane structure on the board to perform frequency or time domain simulations.

Serial Link Design Methodology

When engineers face today's demands for faster data throughput, each section of the interface takes on greater complexity. Transceivers feature dynamic equalization and clock and data recovery algorithms that require advanced modeling techniques. S-parameters for IC package models must be used to accurately characterize interconnect from the die to the package pin. And PCB structures must be carefully characterized such that signal loss, frequency-dependent materials, and impedance discontinuities are all accurately represented through broadband S-parameter interconnect models.

The Allegro PCB SI solution features integrated field solvers (including 2D full-wave FEM), support for the IBIS 5.x algorithmic model interface (AMI) standard for describing SerDes signal processing, and accurate analytical via modeling (narrowband, wideband, s-parameter). Allegro PCB SI is a uniquely integrated and accurate solution for serial link design and compliance testing. It combines the ability to accurately model from die to die, while providing high-capacity (millions of bits) simulation and statistical analysis techniques that ensure electrical compliance of industry-standard protocols such as PCI Express and Serial ATA.

Multi-gigabit serial link designs should follow a front-to-back design flow where pre-route analysis drives constraints that guide physical implementation. The flow continues with routed designs being screened for candidate channels that may be in jeopardy of not meeting compliance specifications. These at-risk signals can be analyzed in detail using the high-capacity (millions of bits) simulation.

Eye diagrams with compliance eye masks along with bathtub curves are among the wave viewer options that engineers have to measure for interface compliance (see Figure 4). Using Allegro PCB SI, engineers can perform serial link analysis more thoroughly and more efficiently than with proprietary tools supplied by semiconductor and SerDes vendors.

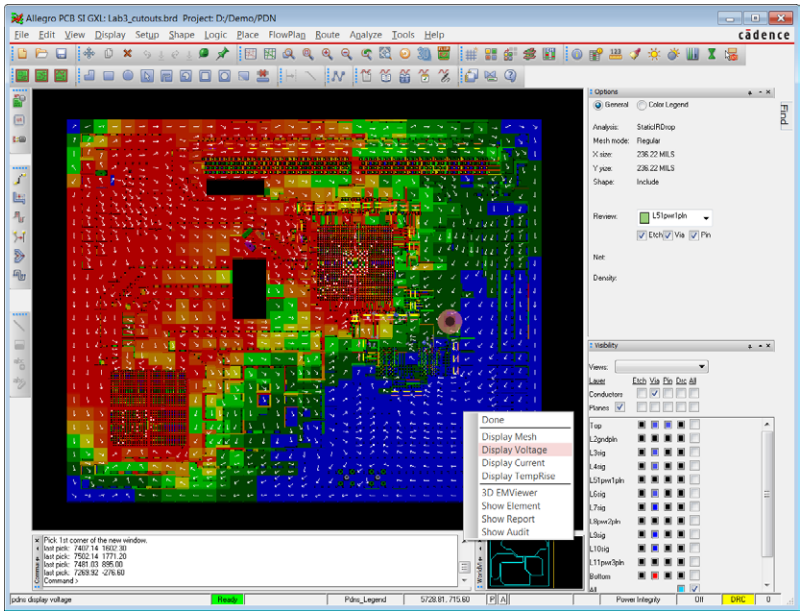

Figure 3: Static IR drop analysis can be performed within the same user interface as signal integrity analysis; engineers can verify power delivery and signal quality from a single environment

Source Synchronous Bus Analysis Methodology

Allegro PCB SI provides a quick and easy methodology to perform post-layout analysis of all the signals associated with a source synchronous bus.

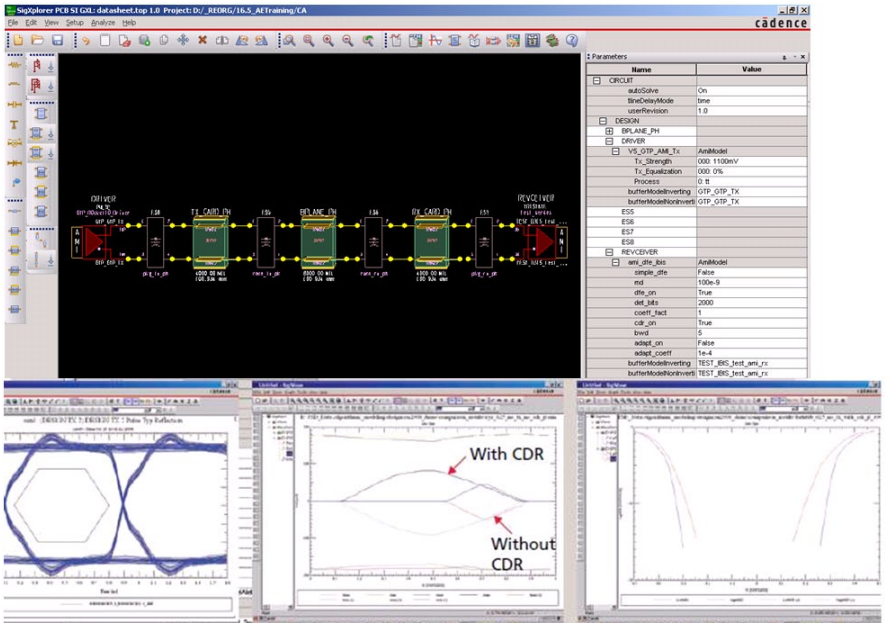

Figure 4: Multi-gigabit serial links can be confirmed to be electrically compliant with interface standards such as PCI Express 2.0 through the use of eye masks, algorithmic transceiver models (IBIS-AMI), and high-capacity (million-bit) simulation

It shortens the time to simulate various configurations (read/write, active, idle) associated with the functioning of source synchronous buses with or without on-die termination (ODT). The Allegro PCB SI solution allows signals to be associated and to save such associations with the design database. Users have a choice of performing reflection analysis or a more comprehensive analysis with crosstalk

included. Allegro PCB SI enables engineers to derate setup and hold margins through user-defined derating tables for different signals in the source synchronous bus (see Figure 5).

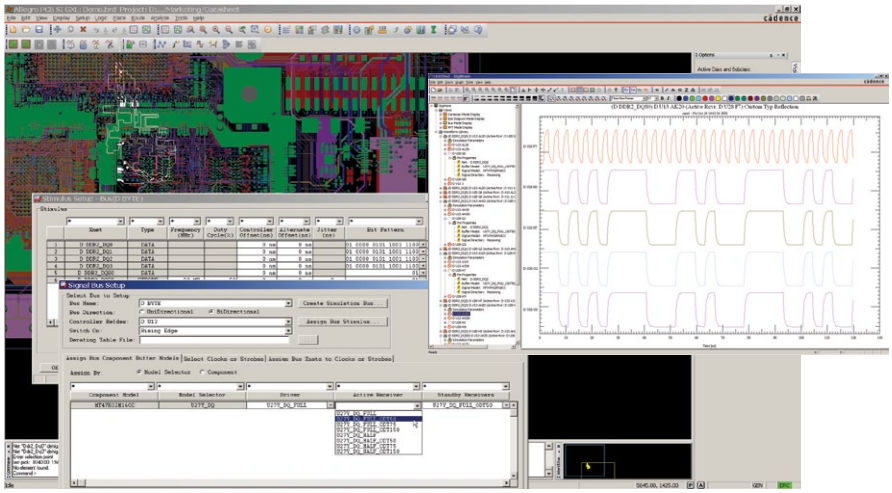

Figure 5: Engineers can validate timing requirements on routed source synchronous signals (i.e. DDR3) through a methodology that prevents unnecessary simulations; efficient post-route bus analysis ensures that critical project deadlines are met

Additional Features

Estimated crosstalk – This feature allows users to reduce the number of required layers by creating crosstalk tables that drive interactive and automatic routing to maintain crosstalk budgets.

Design link (package-board or multi-board) – Interconnects from multiple PCB and IC package designs can be combined using Allegro PCB SI design link technology to analyze die to die through packages, boards, and connectors.

EMI analysis and rulechecking – Single- or coupled-net EMI simulation along with a comprehensive rule-checking engine, EMControl, enables engineers to design for EM compliance.

Model integrity – Users can create, manipulate, and validate models quickly in an easy-to-use editing environment. Support is available for IBIS, Spectre®, Mentor/Quad XTK, and Synopsys HSPICE (requires HSPICE simulator and license, which is not included with Allegro PCB SI).

Resource library – A comprehensive library of technical papers, design-in IP (for example, PCI Express and DDR2), and how-to movies are available by visiting cadence.com (Products and Solutions > PCB Design > Resource Library).

Mentor Board Station flow – A bi-directional interface with the Mentor Board Station enables analysis and routing within Allegro PCB SI, with the final results committed back to the Mentor Board Station environment so that existing manufacturing output processes are preserved.

Operating System Support

Allegro Platform Technology:

- Sun Solaris
- Linux
- IBM AIX
- Windows

ORCAD Technology:

- Windows

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more

For More Information

Contact Cadence sales at 1.800.746.6223 or visit www.cadence.com for additional information. To locate a Cadence sales office or channel partner in your area, visit www.cadence.com/contact_us.

Major Feature Summary for Allegro PCB SI Products

PCB SI product comparison grid (OrCAD, Allegro XL/GXL)	OrCAD PCB SI	Allegro PCB SI XL	Allegro PCB SI GXL
Macro modeling support (DML)	•	•	•
IBIS 5.0 support	•	•	•
IBIS ICM model support	•	•	•
Spectre-to-DML	•	•	•
HSPICE-to-IBIS	•	•	•
Graphical topology editor	•	•	•
Lossy transmission lines	•	•	•
Coupled (3 net) simulation	•	•	•
Differential pair exploration and simulation	•	•	•
Custom stimulus	•	•	•
Topology append	•	•	•
Generate estimated crosstalk tables	•	•	•
Detailed simulation reports	•	•	•
Coupled (>3nets) simulation	•	•	•
Allegro Physical Viewer Plus		•	•
Differential pair extraction from Allegro PCB Designer	•	•	•
Differential pair extraction from Allegro Design Authoring		•	•
Current probes	•	•	•
Multi-terminal black boxes in topologies	•	•	•
Custom measurement	•	•	•
Post-layout selection and crosstalk simulation from Allegro PCB Designer	•	•	•
HSPICE interface	•	•	•
Differential signal constraint capture	•	•	•
Comprehensive simulation	•	•	•
Sweep simulations	•	•	•
Constraint development and capture of topologies	•	•	•
Wide band analytical via model generator	•	•	•
Topology apply		•	•
Constraint-driven floorplanning and placement		•	•
Allegro Constraint Manager		•	•
Color-coded real-time feedback on violations		•	•
Spectre transistor-level model support		•	•
Source synchronous bus analysis		•	•
Batch simulation		•	•
EM Control: rules development		•	•
EM Control: rules checking		•	•
EMI differential simulation		•	•
Constraint-driven routing		•	•
Allegro PCB Router XL		•	•
Static IR drop analysis		•	•
Simultaneous switching noise (SSN) analysis		•	•
S-Parameter DC extrapolation		Multi-Gigabit	•
S-Parameter generation from stack-up		Multi-Gigabit	•
S-Parameter plotting in SigWave		Multi-Gigabit	•
Time domain simulation of S-Parameters		Multi-Gigabit	•

PCB SI product comparison grid (OrCAD, Allegro XL/GXL)	OrCAD PCB SI	Allegro PCB SI XL	Allegro PCB SI GXL
Library management of S-Parameters in model integrity		Multi-Gigabit	•
Coupled via model generator for pre-layout explorations		Multi-Gigabit	•
High-capacity channel simulation		Multi-Gigabit	•
Optimum pre-emphasis bit configurations (“tap settings”)		Multi-Gigabit	•
BER prediction		Multi-Gigabit	•
Bathtub curves		Multi-Gigabit	•
Channel compliance—statistical analysis		Multi-Gigabit	•
Post-layout MGH extraction		Multi-Gigabit	•
Signal quality screening of routed nets		Multi-Gigabit	•
Voltage ripples in time domain		PDN Option	•
Impedance requirements calculator		PDN Option	•
Decoupling capacitor selection and placement		PDN Option	•
VRM editor		PDN Option	•
Decoupling capacitor library editor		PDN Option	•
Cross-probing between waveform and design canvas		PDN Option	•
Frequency domain analysis		PDN Option	•
IC switching currents		PDN Option	•
Package and die parasitics		PDN Option	•

Notes:
PDN Option: Allegro PCB Power Delivery Network Analysis Option
Multi-Gigabit: Allegro PCB SI Multi-Gigabit Option

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Cadence is transforming the global electronics industry through a vision called EDA360. With an application-driven approach to design, our software, hardware, IP, and services help customers realize silicon, SoCs, and complete systems efficiently and profitably. www.cadence.com