Title: Properties – From Capture to PCB Editor

Product: OrCAD Capture, Allegro DE CIS and OrCAD / Allegro PCB Editor

Summary: It explains how to create properties in Capture and how to export them to PCB Editor.

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1 Properties - from Capture to Allegro

1.1 CIS-Properties in Capture

All Properties in the CIS DB can be transferred to the schematic. Some of them are used to make it easier to create a schematic, some are used to export them into a BOM and some are used to transfer them to PCB Editor.

With Property Editor you can see all transferred CIS properties. It’s also possible to change the property values but it makes no sense if you work in a defined property flow.
1.2 Room Properties

The Room Property assigns the part to a specific area or room of the PCB. The detailed description of using a Room property in DE CIS and PCB Editor is part of the basic trainings.

1.3 Net and Electrical Properties

You can define nearly all net rules by adding properties to the nets in the Property Editor of DE CIS. To use electrical rules you need Allegro PCB Editor Performance Option.

Please remember that net and electrical properties overwrite the constraint sets from PCB Editor Constraint Manager. It’s easier to handle rules in constraint manager than as Capture properties.

Some basic properties are shown in the DE CIS Training.

All following property you can use with Allegro PCB Editor. These properties are for net rules not for electrical rules.

**FIXED**

Attached to components, symbols, nets, pins, vias, clines, lines, filled rectangles, rectangles, shapes and groups. To indicate that the object cannot be moved or deleted, the automatic router is not to rip up connections in the net, and that glossing is not to be performed on the net assign a TRUE value.

**MIN_LINE_WIDTH**

This rule attaches to a net and sets the minimum width of a net or line. Use this property to override the Min line width rule in a physical constraint set. It also overrides the Line Width electrical constraint for a differential pair, if set. The value of this property is in design units.

**NO_GLOSS**

This rule attaches to a net and when you assign a TRUE value indicates the net should not be glossed.

**NO_PIN_ESCAPE**

This rule attaches to a reference designator, net, or pin. When a TRUE value is assigned, the Pin Escape Router is not to place pin escapes on this component, net, or pin during routing.

**NO_RAT**

This rule attaches to a net. When a TRUE value is assigned, nets do not display rats nests for unconnected pins.
<table>
<thead>
<tr>
<th>Property</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>NO_RIPUP</td>
<td>This rule attaches to a net. When a TRUE value is assigned, the etch on this net is not to be ripped up (removed) by the automatic router. Any connections on a net added after you assign this property can be ripped up.</td>
</tr>
<tr>
<td>NO_ROUTE</td>
<td>This rule attaches to a net or reference designator (component). When a TRUE value is assigned, missing connections on this net are not routed.</td>
</tr>
<tr>
<td>NO_TEST</td>
<td>This rule attaches to a net. When a TRUE value is signed, test points are not added during test point generation.</td>
</tr>
<tr>
<td>PROBE_NUMBER</td>
<td>This rule attaches to a net. Assign a positive integer to this rule to represents the test probe to be used for testing the net.</td>
</tr>
<tr>
<td>ROUTE_PRIORITY</td>
<td>This rule attach to a net. The positive integer assigned to this rule represents the routing priority for the net. Allegro PCB Editor/APD routes the net according to the priority order. Nets with the lowest number have the highest priority. To identify nets to be routed first, tag those critical nets with a ROUTE_PRIORITY property value of 1.</td>
</tr>
<tr>
<td>SAME_NET</td>
<td>This rule attaches to a net. When a TRUE value is assigned, elements in the same net are checked for spacing violations.</td>
</tr>
<tr>
<td>SHIELD_NET</td>
<td>This property adds a “shield” statement to the “net” statement. The value assigned to this rule is the name of the net used for shielding the net associated to the property. This allows you to control SPECCTRA.</td>
</tr>
<tr>
<td>TS_ALLOWED</td>
<td>This rule attaches to a net and specifies whether T connections can be made and the location of the T connections.</td>
</tr>
<tr>
<td>VIA_LIST</td>
<td>This rule attaches to a net. This rule lists the via names (wildcards allowed) that can be used for connections in this net.</td>
</tr>
<tr>
<td>VOLTAGE</td>
<td>This rule attaches to a net to indicate that the net is a DC net. The value of this property is the voltage of the DC net. For example, a value might be 2.2 V. Nets with the voltage property do not display a rats nest. Unconnected nets with this property are displayed by a boxed X feature rather than a rat to the unconnected pins.</td>
</tr>
</tbody>
</table>
WEIGHT
This rule attaches to a net. It used by automatic placement and automatic gate swapping. The assigned value is an integer between 0 and 100 where a high weight value instructs Allegro PCB Editor/APD to make nets as short as possible. Automatic placement uses the WEIGHT property to keep the components on the net close together.

All following properties can be used with Allegro Performance Option. These properties are for electrical rules. In Allegro PCB Editor XL you can use further properties.

DIFFP_UNCOUPLED_LENGTH
This property replaces DIFFP_2ND_LENGTH and overrides the Max uncoupled length electrical constraint for differential pairs. This rule sets the cumulative maximum distance that segments of one net in a differential pair can run inside or outside the coupling band. The value of this property is in design units.

DRIVER_TERM_VALUE
Attach to a net. The value of a terminator component is not be added to the driver end of the net. Used by the automatic terminator assignment program.

ECL
This property identifies a high speed net with a value of either TRUE or FALSE. Used by automatic routing and rats nest scheduling. If the ECL property is attached to a net, Allegro PCB Editor/ APD assume a stub length of zero and a rats nest schedule of SOURCE_LOAD_DAISY_CHAIN.

EDGE_SENS
This constraint property defines whether or not a receiver is sensitive to non-monotonicity in the waveform. The value of this constraint shows which edges of the waveform are sensitive, that is, rising edge only, falling edge only, both edges, or neither edge.

ELECTRICAL_CONSTRAINT_SET
This property names the electrical constraint set to apply to the net. Any net that does not have an ELECTRICAL_CONSTRAINT_SET property has the default ECSet.

IMPEDANCE_RULE
Specifies an impedance restriction between any two pins on a net or between any pin and Tpoint connection on a net. Used by DRC checking and routing.

MAX_BVIA_STAGGER
Attached to a net, the maximum center-to-center distance between the connect point of one pin or blind/buried via (the pin or via xy location) and the connect point of the other, where the two pins or vias are on the same net and have a single connect line joining them.
MAX_PARALLEL  Attached to a net or connect line. This property overrides the Max parallel electrical constraint. The value is a character string of up to four different lengths and distances. Separate each length-distance value by a colon (:) and each length-distance pair by a semicolon (;).

MIN_BVIA_GAP  This rule attaches to a net and evaluates the minimum center-to-center spacing between the connect points of two buried vias that do not share a common layer.

MIN_BVIA_STAGGER  Attached to a net. The minimum center-to-center distance between the connect point of one pin or via (the xy location of the pin or via) and the connect point of the other, where the two pins or vias are on the same net and have a single connect line joining them.

MIN_HOLD  Used by the Timing Setup/Hold tab of the Allegro Constraint Manager. It defines the minimum hold time of a data signal relative to a clock signal. The value of the property is in nanoseconds and can be attached to either the data net or a pin of the data net.

MIN_SETUP  This rule is used by the Timing Setup/Hold tab of the Allegro Constraint Manager. It defines the minimum setup time of a data signal relative to a clock signal. The value of this property is in nanoseconds and can be attached to either the data net or a pin of the data net.

PROPAGATION_DELAY  This rule defines the minimum and maximum propagation delay constraint between any pair of pins or rat-Ts in a net or an extended net (Xnet). The value assigned to this rule is a string value.

RELATIVE_PROPAGATION_DELAY  This property replaces MATCHED_DELAY in Allegro PCB Editor version 14.0. Electrical constraint attached to pin pairs on a net. Specifies a group of pin pairs that are required to have interconnected propagation delays that match a specified delta (offset0 and tolerance). A RELATIVE_PROPAGATION_DELAY group has one or more reference pin pairs against which all other pin pairs in the group are compared.

TESER_GUARDBAND  This rule is used by the Timing Setup/Hold tab of the Allegro Constraint Manager. It can be used to define a fudge factor for the setup and hold calculation. Assigned values are measured in nanoseconds and can be attached to either a net or a pin of a net where the net is the data net of a timing check.
**TESTPOINT_QUANTITY**

This rule specifies the desired number of test points on the net. When test points are generated automatically using Manufacture-Testprep- Automatic, the number of test points generated do not exceed the number specified. A net with the TESTPOINT_Quantity property has a default value of 1.

**TOPOLOGY_TEMPLATE**

This net attaches to a net. In version 13.6, this rule records the name of the topology template assigned to the net. In version 14.0 this information is recorded as part of an ECSet while the property remains compatible with 13.6 drawings. The value assigned can be upreved to 14.0 ECSet assignments using the Audit-Topology Templates command in the Allegro Constraint Manager.

**TOTALETCH_LENGTH**

Use this property as an override to the constraint by the same name. The value of this property is a string with a format of <min>:<max>, where both <min> and <max> are etch length values with optional units. If no units are specified, the units of the drawing will be assumed. Either value is optional. If only a max value is specified, the leading colon is required. If only a min value is defined, the trailing colon is optional.
1.4 Propref.pdf

In your system folder <CDSROOT>/doc/propref you find the file Propref.pdf. This file contains the detailed description of all properties in the Allegro flow with detailed syntax descriptions and examples.

1.5 Prefprop File for Propertie Editor Filter

In the top row of the Property Editor you can choose a Filter. By default the Filter is set to <Current properties>.

![Property Editor](image)

When you work with net or electrical properties please choose the filter Cadence-Allegro.

![Property Editor](image)

In the system folder <CDSROOT>/tools/capture you find the prefprop.cfg file. This file contains all Filters which are available in the Property Editor Filter selection. You can define your own filter and store the file to a different folder. The path to the prefprop.cfg file is set in the capture.ini file.
1.6 UI for electrical Properties

You have several UIs to define electrical rules. Here is an example how to create Relative Propagation Delay.

1. Double-click the net where you want to assign the PROPAGATION_DELAY property. The Property Editor window appears.
2. Select the Filter as Allegro_Signal_Flow_Routing or Cadence-Allegro.
3. Select the Flat Nets tab. Based on the grid-settings, rows or columns corresponding to different properties appear.
4. Select the grid corresponding to the PROPAGATION_DELAY property.
5. Right-click on the grid corresponding to the PROPAGATION_DELAY property and select the Invoke UI command from the pop-up menu. The Propagation Delay dialog box appears.

Note: You can create all rules by properties in DE CIS but it's much easier to organize all rules in the PCB Editor Constraint Manager. We talk about the CM in the next chapter.
1.7 Allegro.cfg

After finishing the schematic you have to export the netlist. The allegro.cfg file defines which properties are transferred to PCB Editor. The allegro.cfg file is located in <CDSROOT>/tools/Capture.

You can go to this folder and open the allegro.cfg with a text editor or you open it out of DE CIS by following these steps:

Select the design file in the project view.

Select Tools -> Create Netlist -> PCB Editor.
Select Setup.

![Configuration File: FB_16_U\roots\Capture\allegro.cfg Edit...]

You can see the path to allegro.cfg. You can create a global allegro.cfg file and store the file in a read only area of your server. The path to the allegro.cfg file is also stored in the capture.ini.

Select Edit to open the file.

The allegro.cfg file has different blocks of properties.

- **[ComponentDefinitionProps]** Properties which are used to build the device type for the PCB editor netlist. Don’t change this definition after you started with Capture or DE CIS.

- **[ComponentInstanceProps]** All component properties which you want to transfer to PCB Editor in addition to the component definition properties.

- **[netprops]** Net properties for spacing, physical and electrical rules.

- **[functionprops]** A function is a part of a component. These properties are function based.

- **[pinprops]** Pin properties
Example for a allegro.cfg file.

[ComponentDefinitionProps]
ALT_SYMBOLS=YES
CLASS=YES
PART_NUMBER=YES
TOL=YES
VALUE=YES
POWER_GROUP=YES
SWAP_INFO=YES
Power_Pins=YES

[ComponentInstanceProps]
GROUP=YES
ROOM=YES
VOLTAGE=YES

[netprops]
ASSIGN_TOPOLOGY=YES
BUS_NAME=YES
CLOCK_NET=YES
DIFFERENTIAL_PAIR=YES
DIFFP_2ND_LENGTH=YES
DIFFP_LENGTH_TOL=YES
ECL=YES
ECL_TEMP=YES
ELECTRICAL.Constraint_SET=YES
EMC_CRITICAL_NET=YES
IMPEDEANCE_RULE=YES
MATCHED_DELAY=YES
MAX_EXPOSED_LENGTH=YES
MAX_FINAL_SETTLE=YES
MAX_OVERTSHOOT=YES
MAX_VIA_COUNT=YES
MIN_BOND_LENGTH=YES
MIN_HOLD=YES
MIN_LINE_WIDTH=YES
MIN_NECK_WIDTH=YES
MIN_NOISE_MARGIN=YES
MIN_SETUP=YES
NET_PHYSICAL_TYPE=YES
NET_SPACING_TYPE=YES
NO_GLOSS=YES
NO_PIN_ESCAPE=YES
NO_RAT=YES
NO_RIPUP=YES
NO_ROUTE=YES
NO_TEST=YES
PROBE_NUMBER=YES
PROPAGATION_DELAY=YES
RELATIVE_PROPAGATION_DELAY=YES
RATSNEST_SCHEDULE=YES
ROUTE_PRIORITY=YES
SHIELD_NET=YES
SHIELD_TYPE=YES
STUB_LENGTH=YES
SUBNET_NAME=YES
TS_ALLOWED=YES
VOLTAGE=YES
VOLTAGE_LAYER=YES

[functionprops]
GROUP=YES
HARD_LOCATION=YES
NO_SWAP_GATE=YES
NO_SWAP_GATE_EXT=YES
NO_SWAP_PIN=YES
ROOM=YES

[pinprops]
NO_DRC=YES
NO_PIN_ESCAPE=YES
NO_SHAPE_CONNECT=YES
NO_SWAP_PIN=YES
PIN_ESCAPE=YES
1.8 Modify Allegro.cfg

You can add or delete properties to get a company specific list of properties. The properties can be system properties or user defined properties. Many of your properties in the CIS DB are user properties. If the syntax is Property_name=YES the property name and value is transferred to PCB Editor.

When a property name in DE CIS doesn’t match with the property name you need in PCB Editor you can rename a property by using this syntax:

```
SAP_ID=PART_NUMBER
PART_NUMBER=YES
```

SAP_ID is the property name in DE CIS, PART_Number in PCB Editor.