DATASHEET

CADENCE DESIGN CREATION

System designers need to capture design intent quickly to drive physical implementation, and they need the flexibility to collaborate simultaneously with multiple team members. Cadence® design creation technology provides comprehensive, customizable solutions to eliminate risk and accelerate PCB design. It allows schematic designers and layout engineers to work in parallel, supports design reuse, and integrates with digital, analog, and pre-layout signal integrity simulators. With Cadence design creation technology, teams can leverage a constraint-driven flow to retain design intent and reduce design spins.

Cadence design creation technology for advanced PCB systems is available in the following product offerings:

- Cadence Allegro System Architect GXL
- Cadence Allegro Design Entry HDL L and XL

CADENCE DESIGN CREATION TECHNOLOGY

The Cadence Allegro® system interconnect design platform offers complete and scalable technology for the design of PCBs and IC packages. Designs can be created in schematics as well as spreadsheets and HDL (Verilog® language). Tightly integrated with Allegro PCB Editor and the Allegro constraint management system, Cadence design creation technology provides robust and highly customizable solutions for constraint-driven PCB design. It supports enterprise deployment and incorporates a number of features and utilities that accelerate PCB design creation. It also supports design reuse at sheet, block, and design levels in addition to typical copy/paste features. Multiple users can work simultaneously on a design, giving design teams much needed flexibility on time-critical projects. Integration with Cadence Incisive® simulators and Cadence PSpice® simulation enables digital and analog simulation, respectively.

Cadence design creation technology for advanced PCB systems is available in the following product offerings.

- Cadence Allegro System Architect GXL—the industry's first multi-style design creation environment to provide the flexibility and power to create complex system designs using a combination of multiple styles (spreadsheets, traditional schematics, or HDL/Verilog language)
- Cadence Allegro Design Entry HDL L and XL—a complete, scalable, schematic-based solution for creating PCB and IC package schematics

These products enable a constraint-driven flow and provide extensive support for team design and design reuse. Both are tightly integrated with the Allegro constraint management system and the Allegro PCB Editor.

cadence™

BENEFITS

- Shortens time to create designs
- Allows schematic designers and layout engineers to work in parallel
- Reduces design spins via a proven, constraint-driven flow
- Provides special support for net classes, buses, extended nets, and differential pairs
- Reduces rework and prevents errors by supporting flexible design reuse
- Integrates with digital, analog, and pre-layout SI simulators
- Reduces total cost of ownership through enterprise deployment support
- Provides a fully validated flow with Allegro PCB Editor
- Supported by a powerful library creation and management solution
- Offers scalability as complexity grows

FEATURES

CONSTRAINT-DRIVEN DESIGN

Integration with the Allegro® constraint management system makes capturing physical and electrical constraints easy and communication of constraints reliable. In addition to simple nets, the system understands other design objects including net classes, buses, extended nets, differential pairs, and matched groups. It allows reuse of constraints—within and across designs—by using electrical constraint sets (ECSets). Constraint values between the schematic and layout can be compared using Design Differences and changes communicated in either direction. This feature is extremely useful when board layout is outsourced, as constraints are created by design engineers and compliance must be ensured after layout. The spreadsheet-like system allows users to capture all electrical constraints within the design database, eliminating the need to communicate constraints and design data separately. Since the design rule checking (DRC) system in the PCB Editor tracks any constraint violation, the designer can verify that the constraints specified in the schematic database and in the PCB Editor are identical. Advanced features include the ability to automatically extract, use, and override constraints from blocks added to the design. The Allegro platform's constraint-driven flow has been used successfully by customers to reduce design cycles and board spins.

ENTERPRISE DEPLOYMENT SUPPORT

Cadence design creation technology is network-installable and provides support for managed enterprise-wide deployment, lowering total cost of ownership. Default options, menus, and custom utilities can be made available at an installation, site, or at the user level. Administrators can lock any option from being selected using the directive locking utilities. Libraries can be shared at a site level and librarians can employ automated features to make other designers aware of library updates. Scripting and programming language support is also provided, making it easy to deploy organization-specific utilities to all users. Almost all programs and utilities can be run from the command line, making script-based automation possible. All program options can be controlled by the project file, allowing users to launch and run programs from within their customized workflows. Designers can write their own custom rule checks and deploy them.

FLOW VALIDATION

Cadence design creation technology is fully integrated within the Allegro platform to ensure seamless data flow and integration. In contrast to multi-vendor environments, constraint and logic transfer from logical to PCB design, backannotation of data from layout, and many other aspects of the flow are tested routinely and thoroughly with every release. Delivery of advanced capabilities often requires enhancements in multiple tools, and flow validation ensures that these different tools work in synchronization, providing value that can't be matched by point-tool enhancements.

TEAM DESIGN

Cadence design creation technology allows different people on the same project to work simultaneously. A project leader can divide the design between different people and each of them can work on their piece in parallel. The owner of each block is insulated from the changes made by other team members. A team leader chooses to pull-in or integrate the blocks independently. The team leader is automatically informed when team members change blocks, and is given the option to accept/defer acceptance of the changes. This solution provides much needed flexibility for large time-critical projects.

DESIGN REUSE SUPPORT

Most designs start from other designs or reuse significant parts of other designs. Cadence design creation technology gives designers multiple choices for reuse, so they can select the most effective design reuse approach for their design. Sheets from old designs, blocks, or entire designs can be reused, which reduces rework and errors. Engineers can begin a new design using an older design, as seen using the Copy Project utility. Designers can copy single or multiple sheets from one design to another using the Import Sheet UI, or just copy/paste special circuitry between different designs. Designers can reuse electrical constraints as part of a block or by using ECSets.

The technology further allows designers to create reused blocks and place them in a library for use in other designs, just as with components. The connectivity, constraints, and layout from each block can also be reused. The same block can be used multiple times in the same design without renaming or copying.
(See Figure 1.)

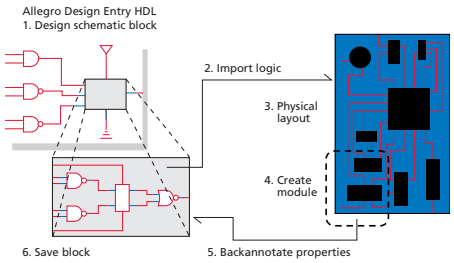

Figure 1: Allegro Design Entry HDL supports full reuse of PCB layout data for hierarchical blocks, increasing reliability and saving time

PUBLISH PDF DOCUMENTATION

(Option available for Allegro Design Entry HDL L/XL)

The Allegro Design Publisher option converts Allegro Design Entry HDL schematics to content-rich Adobe Portable Document Format (PDF) files, creating a secure, single-file representation of the design. The PDF files provide navigation through the hierarchy as well as access to design attributes and constraints, making them ideal for design reviews. Intellectual property (IP) is protected through access controls that allow users to decide what design data is published for review.

SPREADSHEET/TABLE-BASED AUTHORING

(Available in Allegro System Architect GXL only)

Customized for system design, the spreadsheet editor provides many productivity enhancements including powerful sort, filter, search, and copy/paste capabilities. It is available in two viewing modes—component-based view and signal-based view. This allows users to edit the connectivity of multiple components

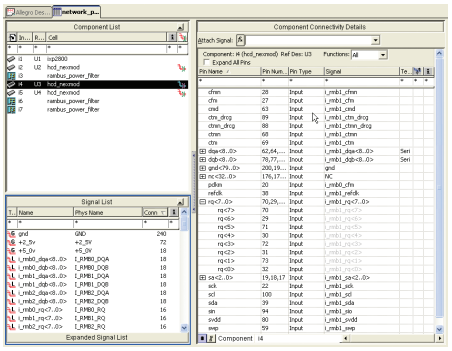

Figure 2: Intuitive spreadsheet editor showing component list, signal list, and connectivity details

at the same time, and it simplifies signal navigation and debugging. It is highly customizable, providing the flexibility to display content and order elements as required. This not only makes editing connectivity for large–pin-count devices much simpler, but designers no longer have to add multiple symbols across many sheets. The spreadsheet editor understands buses, extended nets, and differential pairs natively, which accelerates design. *(See Figure 2.)*

A special matrix view allows users to observe the connectivity of multiple components and signals in a single table. This is ideal, for example, when looking at a specific bus interface. The spreadsheet editor can reduce time capturing connectivity with large–pin-count devices substantially compared to schematic-based mechanisms with observed time savings of up to 80%.

ASSOCIATED COMPONENTS

(Available in Allegro System Architect GXL only)

The large number of discrete components—series and shunt terminators, pull-up/pull-down resistors, and decoupling capacitors—that accompany large-pin-count devices can take a huge amount of time to wire up in a schematic. To make managing these discrete devices easier, Allegro System Architect GXL provides special features to connect and associate them with the large–pin-count devices, and to pass the associations to the PCB Editor. The spreadsheet editor understands special differential terminations in addition to terminations for single-ended nets. The spreadsheet editor automatically detects differential pairs and buses on components, accelerating design with large-pin-count devices.

REPORTS AND SCHEMATIC GENERATION

(Available in Allegro System Architect GXL only)

A report engine provides easy extraction of design information and presents the data in a variety of formats. It

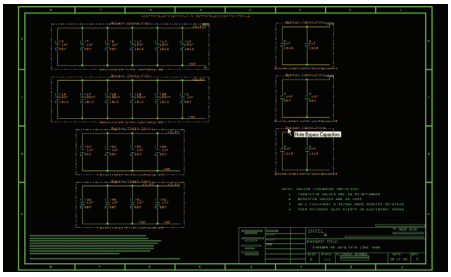

Figure 3: Schematic generator is customized for PCB design with many features such as generating rails for bypass capacitors

allows designers to use existing design relationships in queries and export reports in various formats including HTML, CSV, and tab-separated text. These editable design report files also include the ability to cross-probe to nets and components in the design. The schematic generator has been enhanced to generate compact schematics and allow users to make placement and routing changes in generated schematics, which are preserved for future runs. *(See Figure 3.)*

COMPREHENSIVE UTILITIES

Allegro design creation technology provides a complete array of utilities. They include:

- Part Manager tracks part usage to ensure that parts are always in sync with the design database
- Global Replace searches for parts with specific attributes and replaces them with other parts on a page, set of sheets, on blocks, or in the complete design
- Global Find and Global Navigate make it easy to quickly find a component, pin, or signal anywhere in the design
- Cross-probing with the PCB Editor makes it easy to find components on the PCB by locating them on the schematic and vice versa
- Cross-placement features of the PCB Editor are used to select components in the schematic for placement in the board

- Bill-of-Materials (BOM) Generator can be customized to fit the requirements of any data management system
- Cross-referencer creates cross-reference tables for signals, parts, and pins and appends them to the pages of a design
- Design Differences compares logical and physical designs for netlist, properties, and constraints
- A number of utilities to update the schematic with connectivity changes made on the board
- Project Manager, a customizable tool launcher, allows users to control program options for all tools in the flow
- Build Physical Wizard makes it easy to integrate output from Xilinx, Actel, and Altera FPGAs into PCB designs
- Automatic Table Of Contents (TOC) creation and management speeds schematic documentation
- Allegro Design Publisher can be used to publish Design Entry HDL schematic in Content Rich PDF files, which contain all the design information viewable in any PDF reader
- Variant Editor makes it easy to create multiple variant designs that share the same PCB layout

OPERATING SYSTEM SUPPORT

ALLEGRO PLATFORM TECHNOLOGY:

- Sun Solaris
- Linux
- IBM AIX
- Windows

CADENCE SERVICES AND SUPPORT

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- SourceLink® online customer support gives you answers to your technical questions—24 hours a day, 7 days a week—including the latest in quarterly software rollups, product change release information, technical documentation, solutions, software updates, and more

For more information about this and other products contact:
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