DATASHEET

CADENCE PCB DESIGN: LAYOUT AND ROUTING

Complex physical and spacing constraints, densely packed components, and increasing number of requirements for high-speed signals are just some of the things adding complexity to today's PCB designs. Designers must therefore be able to easily define, manage, and validate simple physical, spacing constraints as well as critical high-speed signals at any stage of the design process. At the same time, they have to ensure that the final PCB meets performance, manufacturing, and test specification goals.

Cadence PCB design solutions are available in the following product suites and options:

- Cadence Allegro PCB Design L, XL, and GXL and options
- Cadence OrCAD PCB Designer, Cadence OrCAD PCB Designer with PSpice, and Cadence OrCAD PCB Designer Basics
- Options for RF PCB Design, Design Partitioning, and Global Interconnect Planning and Routing

CADENCE PCB DESIGN SOLUTIONS

Cadence® PCB design solutions are complete design environments for addressing today's design challenges and manufacturability concerns. The design solutions contain everything needed to take a PCB design from concept to production with a fully integrated design flow, including design capture, component tools, a PCB editor, and an auto/interactive router, as well as interfaces for manufacturing and mechanical CAD. A common database architecture, use model, and library offer complete PCB design solutions for the Cadence OrCAD® and Allegro® product lines, with the scalability to expand as designs and design challenges increase in complexity. The solutions can result in increased productivity, shorter design cycles, and faster ramp up to volume production.

BENEFITS

- Offers a proven, scalable, cost-effective PCB editing and routing solution that can grow as needed
- Provides a complete placement and routing environment—from basic floorplanning, placement, and routing to placement replication, advanced interconnect editing, and strategic global planning and routing
- Eliminates unnecessary iterations through constraint-driven PCB design flow
- Supports a comprehensive rule set for physical, spacing, design for assembly (DFA), high-density interconnect (HDI), and electrical (high speed)
- Features a common, consistent constraint management system for creation, management, and validation of constraints from front to back
- Open environment for third party application improves productivity while providing access to best of breed integrated point tools

cadence™

FEATURES

PCB EDITOR TECHNOLOGY

CONSTRAINT-DRIVEN PCB EDITING ENVIRONMENT

At the heart of Cadence PCB design solutions is a PCB editor—an intuitive, easy-to-use, constraint-driven environment for creating and editing simple to complex PCBs. Its extensive feature set addresses a wide range of today's design and manufacturability challenges:

- A powerful set of floorplanning and placement tools including placement replication for accelerating placement of the design
- PCB design partitioning technology, in the Allegro tiers, provides a concurrent design methodology for faster time to market and reduced layout time
- Powerful shape-based shove, hug interactive etch creation, editing establishes a highly productive interconnect environment while providing real-time, heads-up displays of length and timing margins
- Dynamic shape capability offers real-time copper pour plowing & healing functionality during placement and routing iterations
- PCB RF design option is a complete front-to-back solution, from schematic to layout and manufacturing
- Complete HDI manufacturing rules coupled with constraint-driven design flow provides a Constraint-Driven HDI design flow to accelerate creation of the most challenging HDI designs
- Global Route Environment provides unique technology for strategic planning and routing of complex, highly constrained designs

The PCB editor can also generate a full suite of phototooling, bare-board fabrication, and test outputs, including Gerber 274x, NC drill, and bare-board test in a variety of formats. (See Figure 1.)

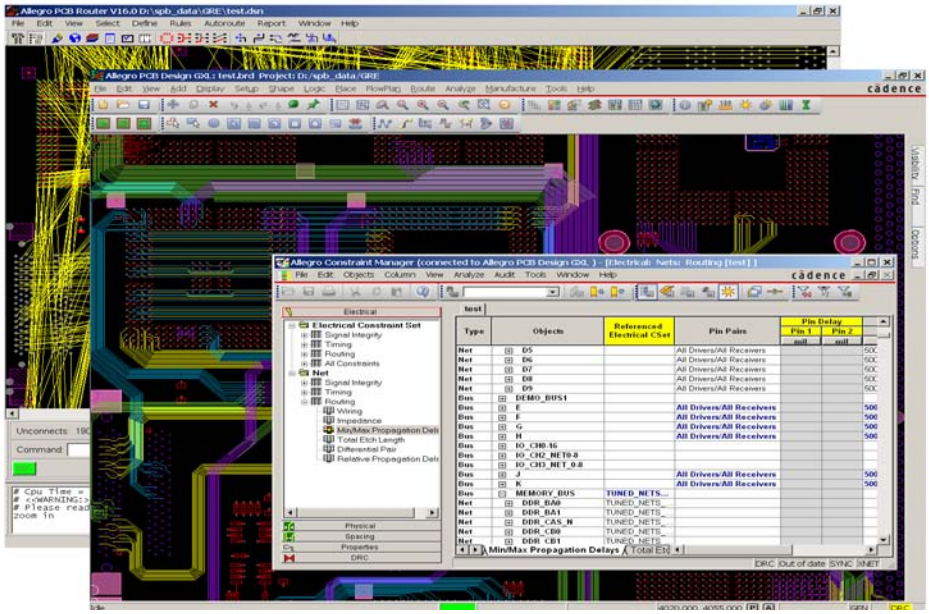

Figure 1: Cadence PCB design solutions bring together all the tools needed to design simple-to-complex PCBs

CONSTRAINT MANAGEMENT

A constraint management system displays physical/spacing and high-speed rules along with their status (based on the current state of the design) in real time and is available at all stages of the design process. Each worksheet provides a spreadsheet interface that enables users to define, manage, and validate the different rules in a hierarchical fashion. With this powerful application, designers can graphically create, edit, and review constraint sets as graphical topologies that act as electronic blueprints of an ideal implementation strategy. Once they exist in the database, constraints can drive the placement and routing processes for constrained signals.

The constraint management system is completely integrated with the PCB editor, and constraints can be validated in real time as the design process proceeds. The result of the validation process is a graphical representation of whether constraints pass (highlighted in green) or fail (highlighted in red). This approach allows designers to immediately see the progress of the design in the spreadsheets, as well as the impact of any design changes.

FLOORPLANNING AND PLACEMENT

The constraint and rules-driven methodology of PCB design solutions includes a powerful and flexible set of placement capabilities, including interactive and automatic. The engineer or designer can assign components or subcircuits to specific "rooms" during design entry or floorplanning. Components can be filtered and selected by reference designator, device package/footprint style, associated net name, part number, or the schematic sheet/page number.

With thousands of components comprising today's boards, precise management is critical. Real-time assembly analysis and feedback can facilitate this management—helping designers increase productivity and efficiency by placing components according to corporate or EMS guidelines. Design-for-assembly (DFA) analysis (available in the Allegro PCB Design XL and GXL tiers) offers this real-time package-to-package clearance checking during interactive component placement. Driven from a two-dimensional spreadsheet array of classes and package instances, real-time feedback provides minimum clearance requirements based on the package's side-to-side, side-to-end, or end-to-end profile. As a result, PCB

designers can simultaneously place devices for optimum routability, manufacturability, and signal timing.

CONSTRAINT-DRIVEN HDI DESIGN FLOW

With BGA pin pitches decreasing to below 1mm—0.8mm or lower with 0.65 or 0.5mm pin pitches—users are forced to implement a buildup PCB technology using high-density interconnect (HDI). While miniaturization is not necessarily the primary objective in many market segments, the move to buildup technology is necessary for fanning out a BGA—particularly if it has three or four rows of pins on each side.

The Allegro constraint-driven HDI design flow provides a proven, robust constraint-driven PCB design flow with a comprehensive set of design rules for all different styles of HDI designs, from a hybrid buildup/core combination to a complete buildup process like ALIVH. In addition, Allegro PCB Editor (XL and above) includes automation for adding HDI to shorten the time to create designs that are correct-by-construction.

STRATEGIC PLANNING AND DESIGN INTENT

Highly constrained, high-density designs dominated by bussed interconnect can take significant time to strategically plan and route. Compound this with the density issues of today's components, new signaling levels, and specific topology requirements—and it's no wonder that traditional CAD tools and technologies fall short of capturing a designer's specific routing intent and acting upon it. The Global Route Environment (available only in Allegro PCB Design GXL) provides the technology and methodology to capture as well as adhere to a designer's intent. Through the interconnect flow planning architecture and the global route engine, users can for the first time put their experience and design intent into a tool that understands what they want—natively.

Users create abstracted interconnect data (through the interconnect flow planning architecture) and can quickly converge on a solution and validate it with the global route engine. The interconnect abstraction reduces the number of elements the system has to deal with—from potentially tens of thousands down to hundreds—resulting in a significant reduction in the manual interaction required. Additionally, users see fewer visual elements in the interconnect flow planning architecture, decreasing the number of elements they must physically manage.

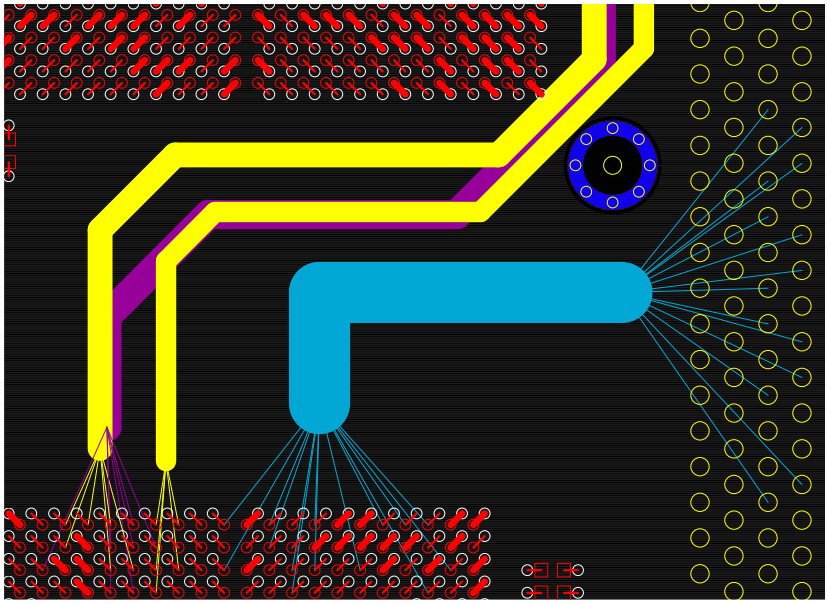

Figure 2: Interconnect flow planning allows users to create route intent using hierarchical flows that can be validated using the route engine to shorten time to route dense, highly constrained PCB designs

Using the abstracted data, the planning and routing process can be accelerated by providing a visual/spatial map of the open area in relation to the data and the user's design intent. The route engine can then deal with the details of the routing, adhering to the specified intent, without the user having to both visualize and solve the interconnect problems at once. This significant simplification over current design tools means users converge on a successful interconnect solution far faster and more easily than ever before, reducing design cycle time through increased efficiency and productivity. (See Figure 2.)

DESIGN PARTITIONING

Globally dispersed design teams are on the rise, which compounds the challenge of shortening design cycle times. Manual workarounds that address multi-user issues are time-consuming, slow, and prone to error.

But PCB design partitioning technology (available in Allegro PCB design tiers) provides a multi-user, concurrent design methodology for faster time to market and reduced layout time. Multiple designers working concurrently on a layout share access to a single database, regardless of team proximity. Designers can partition designs into multiple sections or areas for layout and editing by several design team members. Designs can be partitioned vertically (sections) with soft boundaries or horizontally (layers). As a result, each designer can see all partitioned sections and update the design view for monitoring the status and progress of other users' sections. Such partitioning can dramatically reduce overall design cycles and accelerate the design process.

INTERACTIVE ETCH EDITING

The routing feature of the PCB editor provides powerful, interactive capabilities that deliver controlled automation to maintain user control, while maximizing routing productivity. Real-time, shape-based, any-angle, push/shove routing enables users to choose from "shove-preferred," "hug-preferred," or "hug-only" modes.

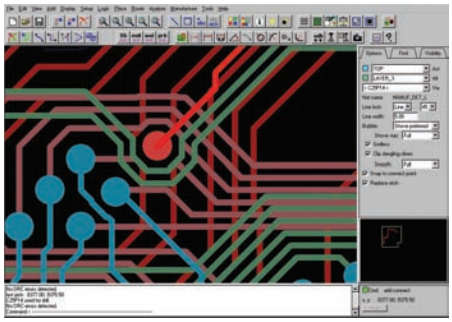

Figure 3: Dynamic push-and-shove capabilities make interactive editing easy on even the most advanced designs

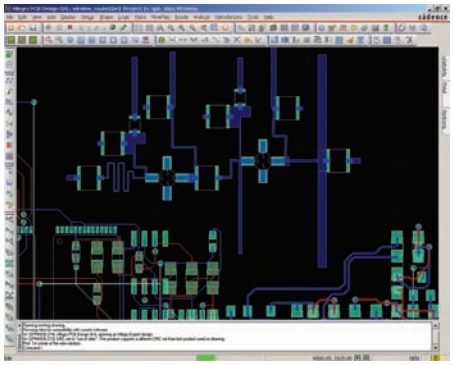

Figure 4: Complete front-to-back solution for PCB RF design

The shove-preferred mode allows users to construct the optimum interconnect path while the real-time, shape-based router takes care of dynamically pushing obstacles. Routes automatically jump over obstacles such as pins or vias. The hug-preferred mode is the perfect solution when a databus needs to be constructed. In hug-preferred mode, the router contour follows other interconnects as a priority and only pushes aside or jumps over obstacles when there is no other option. The hug-only option performs like the hug-preferred mode, but without the push-and-shove aggression on other etch objects. The real-time, embedded, shape-based routing engine optimizes the route by either pushing obstacles or following contours while dynamically jumping over vias or component pins.

During etch editing, the designer can view a real-time, graphical heads-up display of how much timing slack remains for interconnect that has high-speed constraints. Interactive routing also enables group routing on multiple nets and interactive tuning of nets with high-speed length or delay constraints. (See Figure 3.)

DYNAMIC SHAPES

Dynamic shape technology offers real-time copper pour plowing/healing functionality. Shape parameters can be applied at three different levels: global, shape instance, and object-level hierarchies. Traces, vias, and components added to a dynamic shape will automatically plow and void through the shape. When items are removed, the shape automatically fills back in. Dynamic shapes do not require batch autovoiding or other post-processing steps after edits are made.

Design requirements involving high-performance or high-frequency circuits need to be met faster and more accurately than ever before. The RF/mixed-signal technology provides a complete front-to-back solution for PCB RF design—from schematic to layout and manufacturing. RF technology includes advanced RF capabilities, including intelligent layout functionality for parametrically creating and editing RF geometries and a flexible shape editor. A bidirectional Intermediate File Format (IFF) interface provides quick and efficient transfer of RF circuit data for simulation and validation. This bidirectional flow eliminates the manual and error-prone iterations between circuit simulation and layout. (See Figure 4.)

PCB MANUFACTURING

A full suite of phototooling, bare-board fabrication, and test outputs, including Gerber 274x, NC drill, and bare-board test in a variety of formats, can be generated. More important, Cadence supports the industry initiative toward Gerber-less manufacturing through its Valor ODB++ interface that also includes the Valor Universal Viewer. The ODB++ data format creates accurate and reliable manufacturing data for high-quality Gerber-less manufacturing.

PCB AUTOROUTER TECHNOLOGY

PCB routing technologies are tightly integrated with the PCB editor. Through the PCB Router interface, all design information and constraints are automatically passed from the PCB editor. Once the route is completed, all route information is automatically passed back to the PCB editor.

AUTOMATED INTERCONNECT ENVIRONMENT

Increased design complexity, density, and high-speed routing constraints make manual routing of PCBs difficult and time-consuming. The challenges inherent in complex interconnect routing are best addressed with powerful, automated technology. The robust, production-proven autorouter includes a batch routing mode with extensive user-defined routing strategy control as well as built-in automatic strategy capabilities. An interactive routing environment—featuring real-time interactive trace pushing and shoving—helps facilitate quick edits to traces. An interactive placement environment with extensive floorplanning functionality and complete component placement features eliminates the need to switch applications to make placement changes to optimize routing.

By using the auto-interactive floorplanning and placement capabilities, designers can improve routing quality and productivity, which are directly related to component placement. In addition, an extensive rule set allows designers to control a wide range of constraints, from default board-level rules to rules by net/net class and region rules. The high-speed routing features of the Allegro product tiers can handle the net scheduling, timing, crosstalk, layer set routing, and special geometry requirements demanded by today's high-speed circuits.

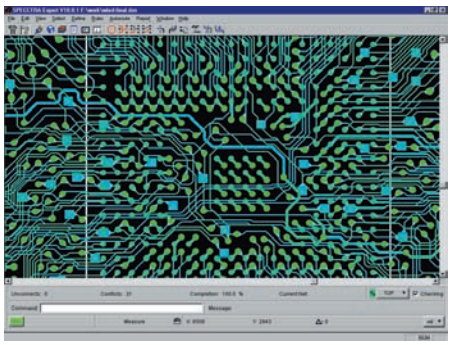

Figure 5: Advanced autorouting technology effectively handles dense, highly constrained designs.

AUTOROUTNG

Advanced autorouting technology provides powerful, shape-based autorouting with fast, high completion rates. Its routing algorithms are designed to handle a wide range of PCB interconnect challenges—from simple to complex, low density to high density—as well as the demands of high-speed constraints. These powerful algorithms make the most efficient use of the routing area. To find the best routing solution for each case, the router uses a multipass, cost-based, conflict resolution algorithm. An extensive rule set enables physical and electrical constraint control, plus has the flexibility to handle specific rules on various routing elements in a design. Users can define rules required for a range of situations, from common physical/spacing net and class rules to complex, hierarchical high-speed rules. (See Figure 5.)

DESIGN FOR MANUFACTURING

The design for manufacturing capability significantly improves manufacturing yields. Manufacturing algorithms provide a spreading capability that automatically increases conductor clearances on a space-available basis. Automatic conductor spreading helps improve manufacturability by repositioning conductors to create extra space between conductors and pins, conductors and SMD pads, and adjacent conductor segments. Users gain the flexibility to define a range of spacing values or to use the default values.

Mitered corners and test points can be added throughout the routing process. The manufacturing algorithms automatically use the optimal setback range, starting from the largest to the smallest value. Test point insertion automatically adds testable vias or pads as test points. Testable vias can be probed on the front, back, or both sides of the PCB, supporting both single side and clamshell testers. Designers have the flexibility to select the test point insertion methodology that conforms to their manufacturing requirements. Test points can be "fixed" to avoid costly test fixture modifications. Test point constraints include test probe surfaces, via sizes, via grids, and minimum center-to-center distance.

HIGH-SPEED CONSTRAINTS

High-speed routing constraints and algorithms handle differential pairs, net scheduling, timing, crosstalk, layer set routing, and the special geometry requirements demanded by today's high-speed circuits. For differential pair routing, users define the gap between the two conductors, and the autorouter takes care of the rest. The routing algorithms intelligently handle routing around or through vias, and automatically conform to defined length or timing criteria. Automatic net shielding is used to reduce noise on noise-sensitive nets. Separate design rules may be applied to different regions of the design; for example, users can specify tight clearance rules in the connector area of a design and less stringent rules elsewhere.

DOCUMENTATION

Cadence tools provide an extensive set of documentation, which includes user guides, context-sensitive help (F1), reference guides, online tutorials, and multimedia demonstrations. The documentation set helps you to:

- Find the answers you need by searching the online help system
- Navigate quickly between related topics with extensive hypertext cross-references
- Learn the tool with the help of the online interactive tutorial
- Find information on error and warning scenarios

OPERATING SYSTEM SUPPORT

Allegro platform technology:

- Sun Solaris
- Linux
- IBM AIX
- Windows

OrCAD technology:

- Windows

CADENCE SERVICES AND SUPPORT

- Cadence application engineers can answer your technical questions by telephone, email, or Internet; they can also provide technical assistance and custom training.
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom.
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet.
- SourceLink® online customer support gives you answers to your technical questions—24 hours a day, 7 days a week—including the latest in quarterly software rollups, product change release information, technical documentation, solutions, software updates, and more.

PCB DESIGN SOLUTIONS COMPARISON GRID
OrCAD, ALLEGRO L, ALLEGRO XL, ALLEGRO GXL SERIES (SPB 16.2)

PCB EDITOR FEATURE SUMMARY	OrCAD PCB DESIGNER/BASICS	ALLEGRO PCB DESIGN L	ALLEGRO PCB DESIGN XL	ALLEGRO PCB DESIGN GXL
Limited database (layers, components, connections)	Basics	n/a	n/a	n/a
Unlimited database	Designer	•	•	•
Netlist/crossplace/crossprobe	•	•	•	•
Padstack and symbol editor	•	•	•	•
Customizable/automated drill legend/NC output	•	•	•	•
Multiple via sizes, blind/buried via support	•	•	•	•
Autoplacement/Quickplace/Floorplanner	•	•	•	•
Dynamic shapes with real-time plowing and healing	•	•	•	•
2-D drafting and dimensioning	•	•	•	•
Multiple UNDO/REDO	•	•	•	•
Gerber 274X, 274D artwork output generation	•	•	•	•
Valor ODB++, ODB++(X) and universal viewer	•	•	•	•
HTML-based reports	•	•	•	•
Exposed copper DRC	•	•	•	•
Interactive routing/etch editing	•	•	•	•
Automatic silkscreen generation	•	•	•	•
Split plane support	•	•	•	•
SKILL runtime, macro, and script support	•	•	•	•
Variant Editor (Design Entry HDL)	n/a	•	•	•
Variant assembly drawing creation	•	•	•	•
Variant bill-of-materials generation	•	•	•	•
CAD interfaces – DXF (Ver.14), IDF (Ver. 2 and 3), IFF import	•	•	•	•
PCB interfaces – PADS (Ver.5), P-CAD (Ver.8), OrCAD Layout	•	•	•	•
Manual testprep	•	•	•	•
Snap enhancements	•	•	•	•
Same Net clearance DRC	•	•	•	•
Via-in-pad rules	•	•	•	•
Stacked via group entity	•	•	•	•
Overlapping Blind/Buried (BB) via support	•	•	•	•
Any layer via support	•	•	•	•
Drill Hole & mechanical pin DRC	•	•	•	•
Non-standard drill support	•	•	•	•
Dynamic Pad Suppression	•	•	•	•
Component alignment		•	•	•
Place Application Mode		•	•	•
Place Alternate symbol		•	•	•
Placement Replication		•	•	•
BB via Stacking allowed		•	•	•
BB via Split / Merge Vias		•	•	•
Technology files		•	•	•
Differential Pair By Region		PCB Performance Option	•	•
Curved Fillet Support		PCB Performance Option	•	•
Length, parallelism, and differential pairs rule support		PCB Performance Option	•	•

PCB DESIGN SOLUTIONS COMPARISON GRID
OrCAD, ALLEGRO L, ALLEGRO XL, ALLEGRO GXL SERIES (SPB 16.2)

PCB EDITOR FEATURE SUMMARY (CONTINUED)	OrCAD PCB DESIGNER/BASICS	ALLEGRO PCB DESIGN L	ALLEGRO PCB DESIGN XL	ALLEGRO PCB DESIGN GXL
Pin-pair multi/matched nested group support		PCB Performance Option	•	•
Real-time DRC and routing of differential pairs and length rules		PCB Performance Option	•	•
Interactive delay tuning		PCB Performance Option	•	•
Complex physical design rule checking (no electrical)		PCB Performance Option	•	•
Group routing		PCB Performance Option	•	•
Measure parasitic		PCB Performance Option	•	•
Advanced trace glossing		PCB Performance Option	•	•
Schematic-driven design reuse modules		PCB Performance Option	•	•
Design-for-assembly rule checking		PCB Performance Option	•	•
Automatic testprep		PCB Performance Option	•	•
Allegro PCB Router high-speed routing alignment (6U)		PCB Performance Option	•	•
Real-time DRC of delay and crosstalk rules		PCB Performance Option	•	•
Constraint regions		PCB Performance Option	•	•
Automatic line width adjustment for impedance rules		PCB Performance Option	•	•
Set, Modify Constraints for existing X-nets		PCB Performance Option	•	•
Layer set rules and routing support		PCB Performance Option	•	•
Via array/shielding		PCB Performance Option	•	•
SKILL development		PCB Performance Option	•	•
Delay, crosstalk, and impedance routing support			•	•
Z-axis delay support			•	•
Extended timing path support			•	•
Group routing (space control)			•	•
Dynamic phase control for differential pairs			•	•
Dynamic design-for-assembly analysis (real-time feedback)			•	•
Display and spread segments over voids			•	•
Back-drilling support			•	•
HDI via span label			•	•
HDI Microvia and associated rules			•	•
HDI Via Stub Report & removal			•	•
HDI via layer transition automation			•	•
Dynamic Fillet generation			•	•
Microvia rules support			•	•

PCB DESIGN SOLUTIONS COMPARISON GRID
OrCAD, ALLEGRO L, ALLEGRO XL, ALLEGRO GXL SERIES (SPB 16.2)

PCB EDITOR FEATURE SUMMARY (CONTINUED)	OrCAD PCB DESIGNER/BASICS	ALLEGRO PCB DESIGN L	ALLEGRO PCB DESIGN XL	ALLEGRO PCB DESIGN GXL
Interconnect data abstraction			Interconnect Flow Designer Option	•
Route engine driven interconnect feasibility analysis and feedback			Interconnect Feasibility Option	•
Global route engine			GRE Option	•
PCB design partitioning technology		PCB Partitioning Option*	PCB Partitioning Option	PCB Partitioning Option
Bi-directional IFF interface			PCB RF Option	PCB RF Option
RF geometry and circuit creation/editing			PCB RF Option	PCB RF Option

PCB ROUTER FEATURE SUMMARY	OrCAD PCB DESIGNER/ BASICS***	ALLEGRO PCB DESIGN L	ALLEGRO PCB DESIGN XL	ALLEGRO PCB DESIGN GXL
6 signal layer limit	•	•	n/a	n/a
256 signal layer limit	n/a	Router Auto/ Interactive Option	•	•
Shape-based or gridded autorouting	•	•	•	•
SMD fanout	•	•	•	•
Trace width by net and net classes	•	•	•	•
Staggered pin support	•	•	•	•
45-degree ECO routing	•	•	•	•
Memory pattern routing (SMD or through-hole)	•	•	•	•
Interactive via search	•	•	•	•
Interactive routing with shoving and plowing	•	•	•	•
Interactive floorplanning	•	•	•	•
Autoplacement	n/a	n/a	•	•
Online design rule checking	•	•	•	•
Flip, rotate, align, push, and move components	•	•	•	•
Placement density analysis	•	•	•	•
Router support for PCB design partitioning files	n/a	•	•	•
Allegro PCB Router ADV 6U or 256U		Router Performance Option**	•	•
Layer set rules and routing support		Router Performance Option**	•	•
Signals on specific layers		Router Performance Option**	•	•
Width and clearance rules by layer		Router Performance Option**	•	•
Via rules by net and/or net class		Router Performance Option**	•	•
Net and/or net class rules by layer		Router Performance Option**	•	•
Crosstalk violation report		Router Performance Option**	•	•
Trace length violation report		Router Performance Option**	•	•
Blind and buried via support		Router Performance Option**	•	•

*PCB Performance Option required
** Router Auto/Interactive required
*** No PCB Router technology is included in the OrCAD PCB Designer Basics suite

PCB DESIGN SOLUTIONS COMPARISON GRID
OrCAD, ALLEGRO L, ALLEGRO XL, ALLEGRO GXL SERIES (SPB 16.2)

PCB ROUTER FEATURE SUMMARY (CONTINUED)	OrCAD PCB DESIGNER/ BASICS***	ALLEGRO PCB DESIGN L	ALLEGRO PCB DESIGN XL	ALLEGRO PCB DESIGN GXL
Via under SMD pad checking		Router Performance Option**	•	•
Automatic wire bonding		Router Performance Option**	•	•
Plural vias		Router Performance Option**	•	•
Stacked vias		Router Performance Option**	•	•
Enhanced via fanout		Router Performance Option**	•	•
Allegro PCB Router DFM 6U or 256U		Router Performance Option**	•	•
Automatic trace spreading		Router Performance Option**	•	•
Automatic via reduction		Router Performance Option**	•	•
Automatic miter 90 to 45		Router Performance Option**	•	•
Automatic test point generation		Router Performance Option**	•	•
Test point specific clearance rules		Router Performance Option**	•	•
Allegro PCB Router HP 6U or 256U		PCB Perfomance Option	•	•
Minimum, maximum, and matched length rules		PCB Perfomance Option	•	•
Crosstalk controls on same and adjacent layers		PCB Perfomance Option	•	•
Virtual pins, which can be moved during autorouting		PCB Perfomance Option	•	•
Parallelism controlled by length and gap		PCB Perfomance Option	•	•
Differential pair routing		PCB Perfomance Option	•	•
Automatic net shielding		PCB Perfomance Option	•	•
Design rules by area		PCB Perfomance Option	•	•
Online display of length tolerance		PCB Perfomance Option	•	•
Global violation indicator		PCB Perfomance Option	•	•
Dynamic display of available length		PCB Perfomance Option	•	•
Automatic single net routing		PCB Perfomance Option	•	•
Multiple net/bus routing		PCB Perfomance Option	•	•
Relative delay rules		PCB Perfomance Option	•	•
Z-Axis delay support (PCB Editor integration)		PCB Perfomance Option	•	•

** Router Auto/Interactive required

*** No PCB Router technology is included in the OrCAD PCB Designer Basics suite

PCB DESIGN SOLUTIONS COMPARISON GRID
OrCAD, ALLEGRO L, ALLEGRO XL, ALLEGRO GXL SERIES (SPB 16.2)

PCB ROUTER FEATURE SUMMARY (CONTINUED)	OrCAD PCB DESIGNER/ BASICS***	ALLEGRO PCB DESIGN L	ALLEGRO PCB DESIGN XL	ALLEGRO PCB DESIGN GXL
Extended timing path support (PCB Editor integration)		PCB Perfomance Option	•	•
Pin-pair multi/matched nested group support (PCB Editor integration)		PCB Perfomance Option	•	•

FRONT-END OPTIONS SUMMARY	OrCAD PCB DESIGNER/BASICS	ALLEGRO PCB DESIGN L	ALLEGRO PCB DESIGN XL	ALLEGRO PCB DESIGN GXL
Allegro Design Entry HDL-or-Allegro Design Entry CIS	OrCAD Capture	•	•	•
Constraint Manager (Allegro Design Entry HDL only)	n/a	n/a	•	•
Part Developer/Component Management	CIS Option	•	•	•
Allegro Design Entry HDL Rules Checker	n/a	n/a	•	•

CONSTRAINT MANAGER FEATURE SUMMARY	OrCAD PCB DESIGNER/BASICS	ALLEGRO PCB DESIGN L	ALLEGRO PCB DESIGN XL	ALLEGRO PCB DESIGN GXL
Physical, Spacing, Proprties, SameNet rules and DRC worksheet	•	•	•	•
Routing rules worksheet		PCB Performance Option	•	•
Region based rules worksheet		PCB Performance Option	•	•
Electrical rules worksheet			•	•

*** No PCB Router technology is included in the OrCAD PCB Designer Basics suite

For additional information, contact Cadence sales at:

+1.408.943.1234

or log on to:

www.cadence.com/ contact_us

cadence™

Cadence Design Systems, Inc.

CORPORATE HEADQUARTERS
2655 Seely Avenue
San Jose, CA 95134
P: +1.800.746.6223 *(within US)*
+1.408.943.1234 *(outside US)*
F: +1.408.943.5001
www.cadence.com

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