

VIRTUOSO XL LAYOUT EDITOR

Virtuoso® XL Layout Editor is the high-end custom block authoring physical layout tool of the Virtuoso custom design platform. It supports the physical implementation of custom digital, mixed-signal, and analog designs at the device, cell, and block level.

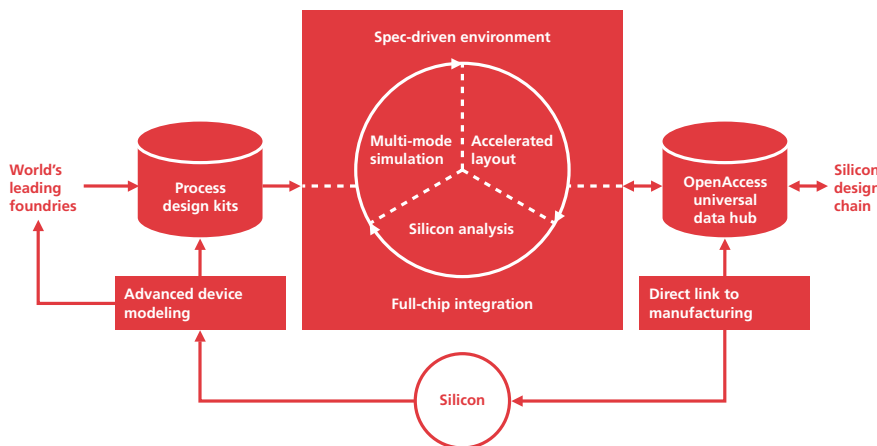


Figure 1: Virtuoso custom design platform

VIRTUOSO CUSTOM DESIGN PLATFORM

The Virtuoso custom design platform is a comprehensive system for fast, silicon-accurate design and is optimized to support “meet-in-the-middle” design methodologies such as advanced custom design. Virtuoso includes the industry’s only specification-driven environment, multi-mode simulation with common models and equations, vastly accelerated layout, advanced silicon analysis for 0.13 microns and below, and a full-chip, mixed-signal integration environment. The Virtuoso platform is available on the Cadence® CDBA database and the industry-standard OpenAccess database. With the Virtuoso platform, design teams can quickly design silicon that is right and on time at process geometries from one micron to 90 nanometers and beyond.

VIRTUOSO XL LAYOUT EDITOR

Virtuoso XL Layout Editor provides accelerated features beyond the basic and mid-range polygon layout features of Virtuoso Layout Editor and Virtuoso Layout Editor Turbo. It supports custom digital, mixed-signal, and analog designs at the device, cell, and block levels. These features provide accelerated connectivity-, constraint-, and design rule-driven functionality with accelerated automation to speed custom block authoring. It includes device generation and editing, block floorplanning, automatic placement, and interactive wire editing in a hierarchical multi-window environment, with parameterized cell (Pcells) and SKILL programming support.

BENEFITS

- Accelerated block authoring through connectivity-driven features and flow (schematic or netlist) promotes a correct-by-construction LVS-correct layout to reduce verification iterations (see Figure 2)
- Increased productivity and design quality with constraint- and design rule-driven features automatically ensure real-time design and process correctness
- Simplified, optimized device generation with the new menu-driven QuickCell (QCell) feature or the standard SKILL programmable Pcells
- Efficiently planned, placed, and routed large block designs with custom floorplanning, automatic placement, and accelerated interactive routing features

FEATURES

CONNECTIVITY-DRIVEN FUNCTIONS AND FLOW

Virtuoso XL Layout Editor has set the standard and changed the way custom block authoring is done. Driven by a schematic connectivity source using Virtuoso Schematic Editor or a netlist source such as CDL or SPICE, an LVS-correct layout can be done in real-time to promote correct-by-construction layout, improved productivity, and reduced verification time.

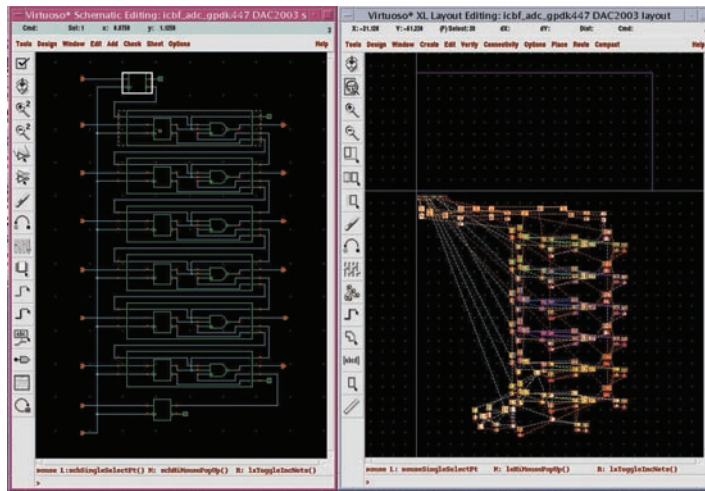


Figure 2: Connectivity-driven LVS-correct layout using Virtuoso Schematic Editor or netlist input

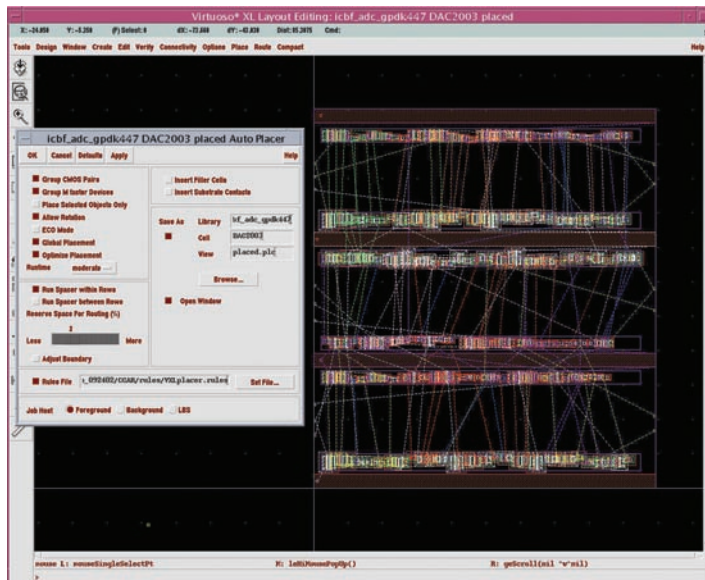


Figure 3: Automatic placement significantly increases design productivity and accuracy

Tedious design tasks, such as device generation, placement, and routing, can be automated (see Figure 3). Schematic and layout can be cross-probed to highlight instances and devices and quickly identify unconnected nets.

CONSTRAINT- AND DESIGN RULE-DRIVEN FUNCTIONS

Virtuoso XL Layout Editor provides design constraint specification and management, and design rule-driven features that are automatically flagged when in violation or enforced in real-time. Coupled with connectivity, this promotes correct-by-construction layout to improve productivity and

reduce physical verification iterations and time. Device generation, placement and routing function constraints, and all technology file process rules are supported including complex 90 nanometer and below.

ACCELERATED LAYOUT AUTOMATION

Virtuoso XL Layout Editor simplifies and optimizes block authoring with accelerated layout automation features that leverage the aforementioned design rule-driven functions and flow. Menu-driven Pcells, QCells, or SKILL programmable Pcells simplify and optimize device generation and editing. Floorplanning and automatic placement simplifies and optimizes the design

planning and location of devices. Accelerated shape-based constraint- and design rule-driven routing simplifies and optimizes the tedious interconnect task (see Figure 4).

SPECIFICATIONS

LAYOUT CREATION AND EDITING

- Includes all Virtuoso Layout Editor and Virtuoso Layout Editor Turbo features (see datasheets)
- Virtuoso Schematic Editor or netlist-driven hierarchical layout
- Interactive Pick-From-Schematic or automated Gen-From-Source device selection
- Menu-driven QCell or SKILL programmable automated device generation
- Automated device editing including abutment, pin permutation, folding, chaining, and cloning (see Figure 5)
- Menu-driven or programmable multi-part path (MPP) feature for guard rings, slotting, etc.
- Design rule-driven editing with real-time notification or enforcement of process rules
- Dynamic measurement
- Constraint-driven specification, management, and real-time notification or enforcement
- Block floorplanning with support rectilinear blocks, pin optimization, and template support (see Figure 6 on next page)
- Automatic constraint and design rule-driven placement of pins, devices, cells, and blocks
- Accelerated shape-based constraint- and design rule-driven interactive routing
- Bi-directional interfacing to Virtuoso Schematic Editor and Virtuoso Chip Assembly Router (see Figure 7 on next page)
- ECO support
- Legacy non-connectivity design importing and connectivity mapping
- Diva® and Assura™ physical verification support

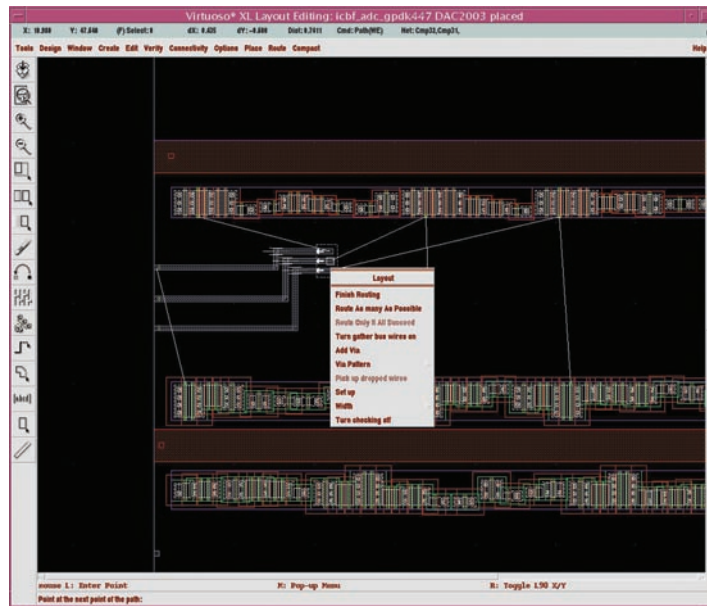


Figure 4: Connectivity, constraint- and design rule-driven interactive routing provides accelerated and accurate block interconnect

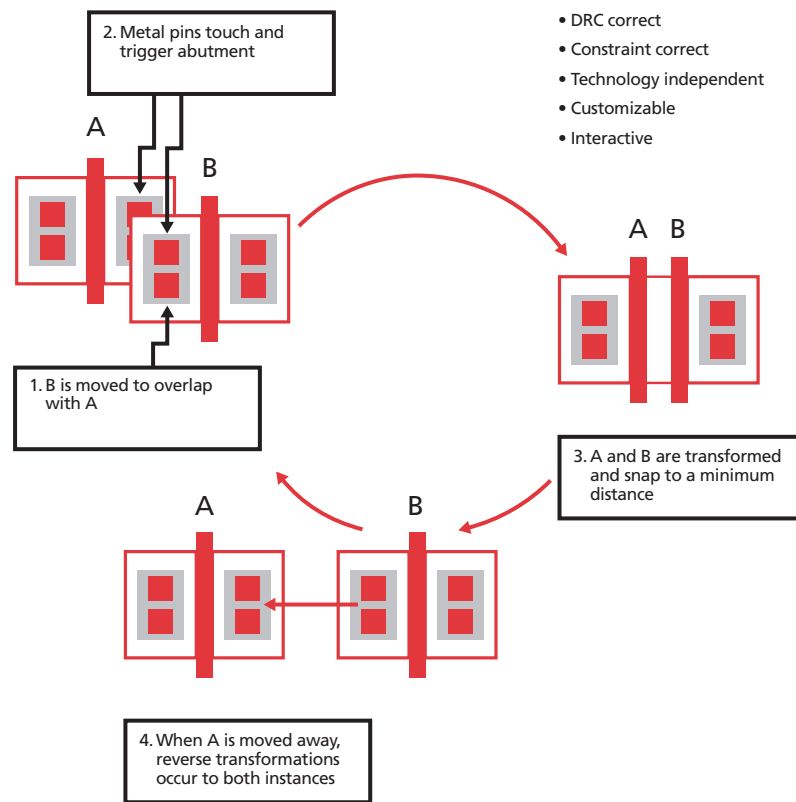


Figure 5: Virtuoso XL Layout Editor automatic abutment (auto-abutment)

DESIGN INPUTS

- Cadence CDBA database
- SKILL
- STREAM format
- OpenAccess database
- Virtuoso Schematic Editor
- CDL and SPICE netlist format
- Virtuoso Chip Assembly Router database format

DESIGN OUTPUTS

- Cadence CDBA database
- SKILL
- STREAM format
- OpenAccess database
- Virtuoso Chip Assembly Router database format

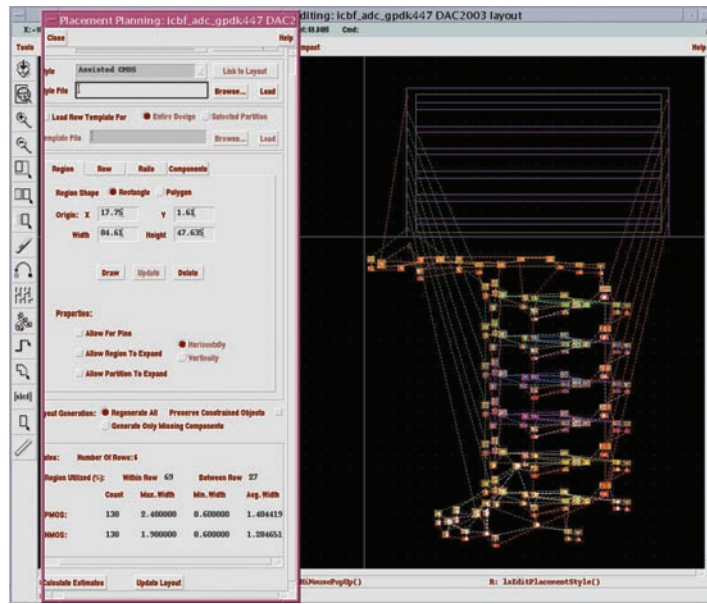


Figure 6: Floorplanning accelerates and ensures the accuracy of design placement and routing

PLATFORM/OS

- Sun/Solaris
- HP-UX
- IBM AIX
- Linux

THIRD-PARTY SUPPORT

- SKILL based tools and functions
- OpenAccess tools and functions
- Process Design Kits (Please reference the PDK datasheets for more information)

CADENCE SERVICES AND SUPPORT

- Customer-focused solutions that increase ROI, reduce risk, and achieve your design goals faster
 - Collaborative approach and design infrastructure—virtual teaming
 - Proven methodology and flow tuned to your design environment
 - Design and EDA implementation expertise
- Product and flow training to fit your needs and preferred learning style
 - Over 80 instructor-led courses—certified instructors, real world experience
 - More than 25 Internet Learning Series (iLS) online courses

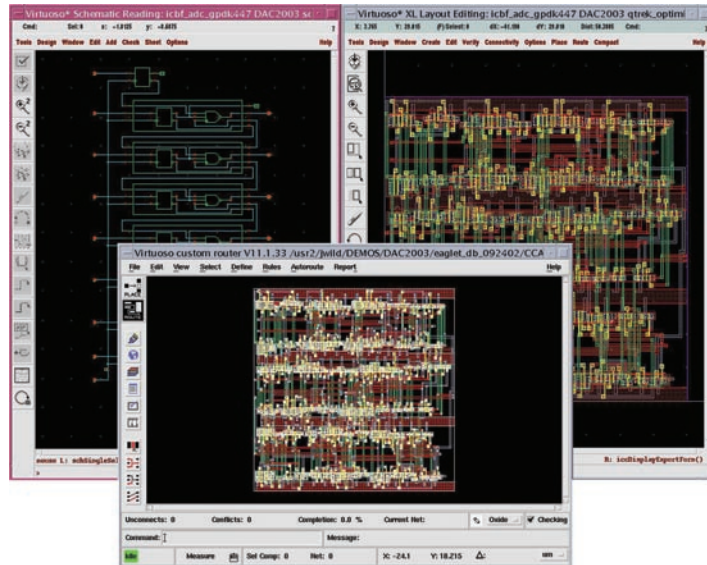


Figure 7: Optional Virtuoso Chip Assembly Router option for fast and accurate automatic interconnect

- Cadence customer support that keeps your design team productive
 - Cadence applications engineers provide technical assistance
 - SourceLink® online support gives you access to software updates, technical documentation, and more—24 hours a day, seven days a week

FOR MORE INFORMATION

Email us at info@cadence.com, or log on to www.cadence.com

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