

VIRTUOSO ULTRASIM

FULL-CHIP FASTSPICE SIMULATOR

Virtuoso® UltraSim Full-chip Simulator is the Cadence® FastSPICE circuit simulator that addresses the need for speed, capacity, design abstraction, and accuracy when verifying your large custom, analog, and mixed-signal designs. Virtuoso UltraSim is an integral part of Virtuoso Multi-mode Simulation, providing all of the simulation components necessary for validating your IC or system.

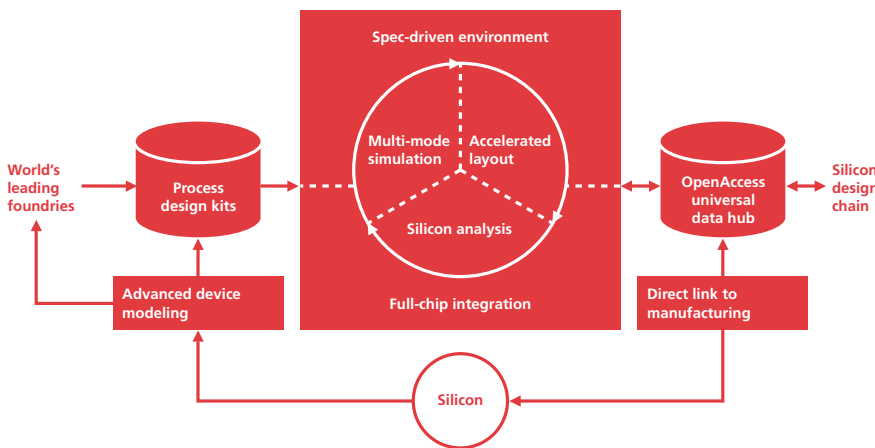


Figure 1: Virtuoso custom design platform

VIRTUOSO CUSTOM DESIGN PLATFORM

The Virtuoso custom design platform is a comprehensive system for fast, silicon-accurate design and is optimized to support “meet-in-the-middle” design methodologies such as advanced custom design. The Virtuoso platform includes the industry’s only specification-driven environment, multi-mode simulation with common models and equations, vastly accelerated layout, advanced silicon analysis for 0.13 microns and below, and a full-chip, mixed-signal integration environment. The Virtuoso platform is available on the Cadence CDBA database and the industry-standard OpenAccess database. With the Virtuoso platform, design teams can quickly design silicon that is right and on time at process geometries from one micron to 90 nanometers and beyond.

VIRTUOSO ULTRASIM

Virtuoso UltraSim is a high-performance transistor-level simulator targeting memories, analog mixed-signal, large custom digital, and SoC designs. It uses true hierarchical simulation with patented isomorphic and adaptive partitioning algorithms to provide the capacity, accuracy, and speed required for design and verification, regardless of design type or stage in your design cycle.

BENEFITS

- Accelerated simulation for a wide range of applications from blocks to complete SoCs
- Design verification flexibility through various modes within Virtuoso UltraSim
- Silicon-accurate simulation by tying Virtuoso Multi-mode Simulation to Virtuoso Advanced Device Modeling, which share the same equations and device models
- Flexibility to switch between environments for different design stages with integration into the Virtuoso Analog Design Environment
- High analog capacity and simulation speed for AMS simulation solutions for block authoring and final verification

FEATURES

COMPATIBILITY WITH SPICE, VIRTUOSO SPECTRE CIRCUIT SIMULATOR, VERILOG-A, DSPF, AND SPEF

Virtuoso UltraSim simulator is compatible with most types of SPICE input decks for both pre- and post-layout. Additionally, it can natively read Virtuoso Spectre® format netlists and models, uses the same views within Virtuoso Analog Design Environment, making it really easy to adopt in Virtuoso Spectre-based design flows.

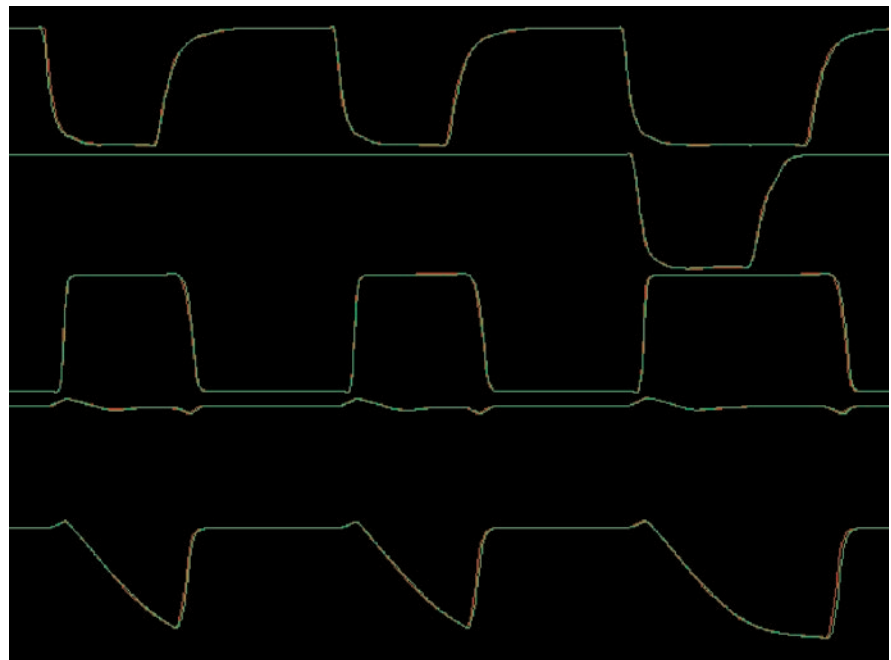


Figure 2: Virtuoso UltraSim vs. SPICE for DRAM slice

POST-LAYOUT SIMULATION

When used in conjunction with Cadence post-layout tools, Virtuoso UltraSim provides a means for exploration and validation of such effects as IR drop, signal integrity, and substrate degradation. Virtuoso UltraSim has built-in, state-of-the-art, S-parameter-based RC reduction for faster simulation with minimal loss in accuracy.

AMS SIMULATION

The Virtuoso UltraSim FastSPICE solver is available inside the AMS simulation technology. It is provided in a use model to enable mixed-signal final verification. In addition, a co-simulation solution with the Verilog-XL simulator is available inside the Virtuoso Analog Design Environment to provide the performance for today's mixed-signal block authoring needs.

DESIGN RELIABILITY

Virtuoso UltraSim has a robust set of analyses capable of predicting and validating timing, power, and reliability. It is the only FastSPICE simulator capable of simulating hot carrier injection (HCI) and negative bias temperature instability (NBTI) — key stress effects that must be taken into account for either high-performance or DSM designs.

SILICON-ACCURATE MODELING

Virtuoso UltraSim, Virtuoso Spectre Circuit Simulator, and Virtuoso Device Modeling share a common set of device models that provide consistent results between all tools. Using the same equations in the simulators and device modeling tools means getting the same results with simulation that are validated during model generation from silicon. This ensures silicon accuracy throughout the design cycle and close correlation in results between SPICE and FastSPICE (Figure 2).

SPECIFICATIONS

DESIGN INPUTS

- SPICE netlist
- Virtuoso Spectre netlist
- DSPF/SPEF
- Verilog®-A
- Virtuoso UltraSim/Verilog
 - Verilog-HDL IEEE 1364
 - PLI 1.0, VPI (PLI 2.0)
 - SDF
- AMS-Virtuoso UltraSim
 - Verilog-HDL IEEE 1364
 - VHDL IEEE 1076
 - Verilog-AMS netlist
 - PLI 1.0, VPI (PLI 2.0)
 - SDF
 - System C, SystemVerilog

DEVICE MODELS

- MOSFET models, including BSIM 1, 2, and 3, with approved versions of BSIM3v3 (3.2.1 and 3.2.2) and BSIM4 from the Compact Modeling Council; high-voltage MOS (HVMOS), MOS9, MOS11, and EKV; mature models for MOS 1, 2, and 3; and specialized switch-level MOS0
- Bipolar junction transistor (BJT) models, including VBIC, HICUM, HBT (for SiGe), Gummel-Poon, and Ebers-Moll models
- Diode models used for either junction or Schottky Barrier diodes with reverse breakdown
- GaAs metal semiconductor field-effect transistor (MESFET), a completely symmetrical model (developed by Statz, Newmann, Smith, Pucel, and Haus)
- Silicon on insulation (SOI), including the Berkeley Technology Associates (BTA) SOI model and the University of California, Berkeley partially-depleted BSIM3SOI model
- Rensselaer Polytechnic Institute's Poly and Amorphous Silicon Thin-Film (TFT) models
- Junction field effect transistor models of various levels
- Specialized reliability models (AgeMOS) for HCI and NBTI modeling
- All models using identical equations as those used for Virtuoso Spectre simulator

DESIGN OUTPUTS

- SST2 waveform format
- PSF waveform format
- ASCII text

PLATFORM/OS

- Sun/Solaris (32- and 64-bit)
- HP-UX (32- and 64-bit)
- Linux

CADENCE SERVICES AND SUPPORT

- Customer-focused solutions that increase ROI, reduce risk, and achieve your design goals faster
 - Collaborative approach and design infrastructure—virtual teaming
 - Proven methodology and flow tuned to your design environment
 - Design and EDA implementation expertise
- Product and flow training to fit your needs and preferred learning style
 - More than 80 instructor-led courses—certified instructors, real-world experience
 - More than 25 Internet Learning Series (iLS) online courses
- Cadence customer support that keeps your design team productive
 - Cadence applications engineers provide technical assistance
 - SourceLink® online support gives you access to software updates, technical documentation, and more—24 hours a day, seven days a week

FOR MORE INFORMATION

Email us at info@cadence.com, or log on to www.cadence.com

