

## VIRTUOSO LAYOUT EDITOR TURBO

Virtuoso® Layout Editor Turbo is the mid-range custom block-authoring physical layout tool of the Cadence® Virtuoso custom design platform. It supports the physical implementation of custom digital, mixed-signal, and analog designs at the device, cell, and block level.

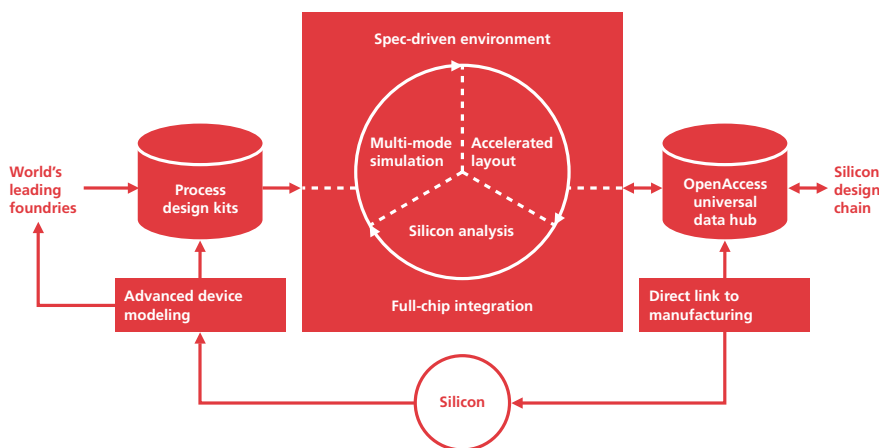


Figure 1: Virtuoso custom design platform

### VIRTUOSO CUSTOM DESIGN PLATFORM

The Virtuoso custom design platform is a comprehensive system for fast, silicon-accurate design and is optimized to support “meet-in-the-middle” design methodologies such as advanced custom design. The Virtuoso platform includes the industry’s only specification-driven environment, multi-mode simulation with common models and equations, vastly accelerated layout, advanced silicon analysis for 0.13 microns and below, and a full-chip, mixed-signal integration environment. The Virtuoso platform is available on the Cadence CDBA database and the industry-standard OpenAccess database. With the Virtuoso platform, design teams can quickly design silicon that is right and on time at process geometries from one micron to 90 nanometers and beyond.

## VIRTUOSO LAYOUT EDITOR TURBO

Virtuoso Layout Editor Turbo provides an intermediate level of accelerated layout features beyond the basic polygon layout features of Virtuoso Layout Editor to increase productivity. Accelerated layout features are bundled with this product to accelerate custom block authoring. They include: QuickCell (QCell), design-rule-driven editing, layout optimization, dynamic measurement, mark net, and alignment. These features all work within in a hierarchical multiwindow environment, with parameterized cell (Pcell) and SKILL programming support.

### BENEFITS

- Simplifies and optimizes device generation using a new menu-driven QCell feature (see Figure 2) or with the standard SKILL programmable Pcells
- Increases productivity and design quality with design-rule-driven features to automatically ensure process design rule correctness in realtime
- Accelerates block authoring tasks with layout automation features including dynamic measurement, alignment, mark net, and point-to-point routing

### FEATURES

#### AUTOMATED MENU-DRIVEN DEVICE GENERATION WITH QCELL

Virtuoso Layout Editor Turbo accelerates the creation and editing of devices with the new QCell menu-driven Pcell feature. The QCell feature eliminates the need for SKILL programming of Pcells and simplifies the installation, creation, and editing process of devices. QCells are C-based, which improves tool performance. SKILL programmable Pcells are an option and are compatible with QCells.

#### DESIGN-RULE-DRIVEN FUNCTIONS

Virtuoso Layout Editor Turbo provides design-rule-driven features that are automatically flagged when in violation or enforced in realtime. This promotes correct-by-construction

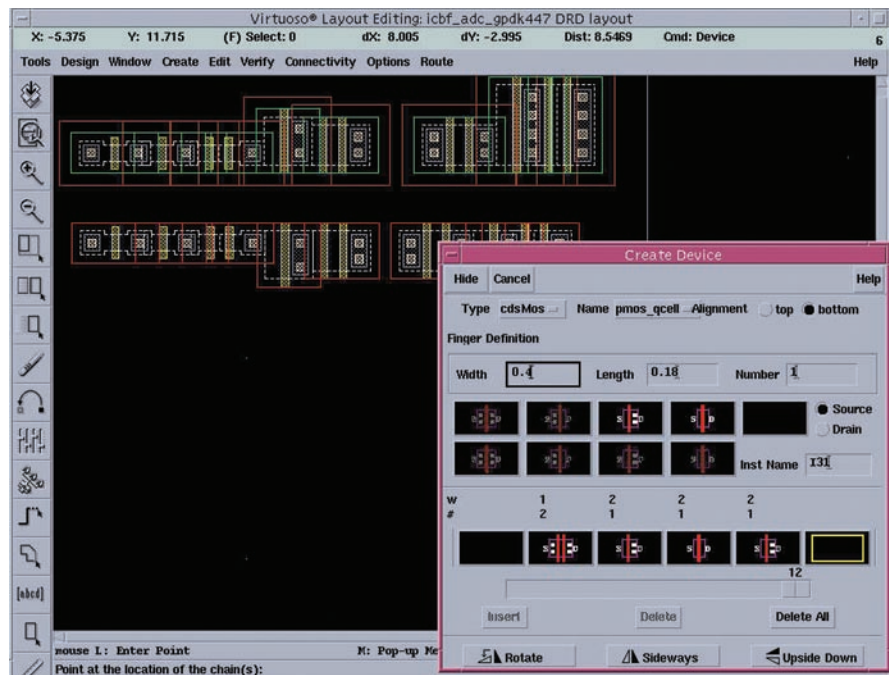


Figure 2: QCell feature accelerates device creation, editing, and placement

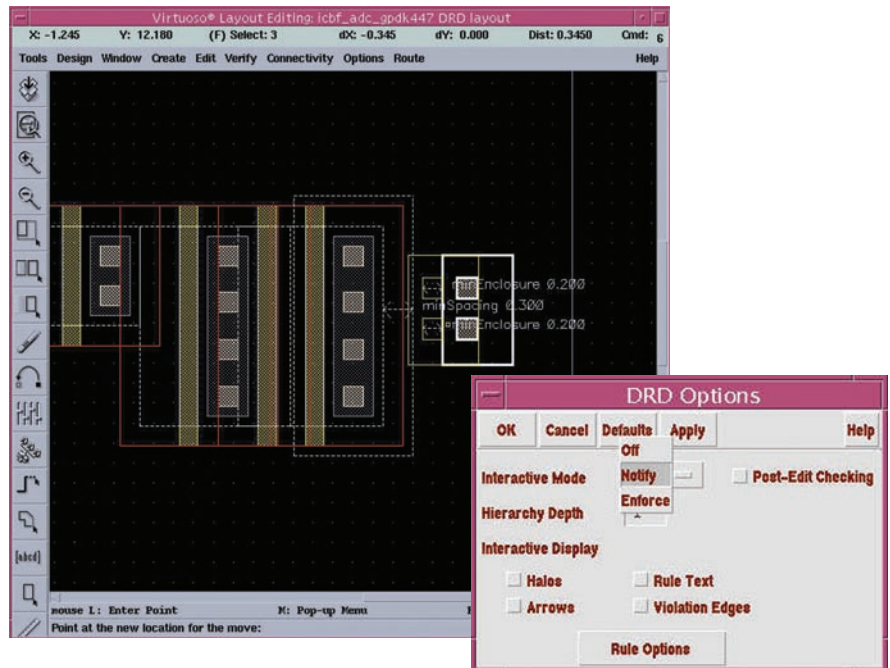


Figure 3: Design-rule-driven editing for fast accurate layout

layout to improve productivity by reducing physical verification iterations and time. All technology file process rules are supported, including complex processes at 90 nanometers and below.

#### ACCELERATED LAYOUT AUTOMATION

Virtuoso Layout Editor Turbo simplifies and optimizes block authoring with accelerated layout automation features

that leverage the design-rule-driven functions and flow (see Figure 3).

- Dynamic measurement minimizes the need to manually measure geometries
- Alignment speeds up the task of aligning instances, pins, and objects
- Mark net efficiently traverses the physical design hierarchy and performs continuity checking and highlighting

- Hierarchical layout optimization enables quick and easy creation of area-efficient layout

## SPECIFICATIONS

### LAYOUT CREATION AND EDITING

- Includes all Virtuoso Layout Editor features (see datasheet)
- Menu-driven QCell or SKILL-programmable automated device generation
- Design-rule-driven editing with realtime notification or enforcement of process rules
- Dynamic measurement (see *Figure 4*)
- Hierarchical layout optimization
- Automated alignment feature (see *Figure 5*)
- Mark net continuity checking and highlighting (see *Figure 6* on next page)
- Physical verification support with Cadence Diva® and Assura™ tools

### DESIGN INPUTS

- Cadence CDBA database
- SKILL
- STREAM format
- OpenAccess database

### DESIGN OUTPUTS

- Cadence CDBA database
- SKILL
- STREAM format
- OpenAccess database

### PLATFORM/OS

- Sun/Solaris
- HP-UX
- IBM AIX
- Linux

### THIRD-PARTY SUPPORT

- SKILL-based tools and functions
- OpenAccess tools and functions
- Process design kits (please reference the PDK datasheets for more information)

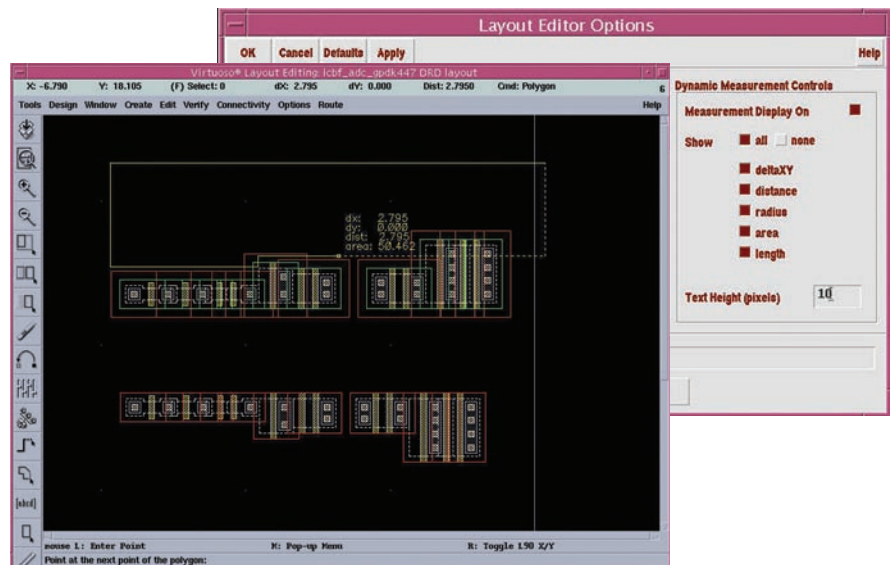


Figure 4: Dynamic measurement enables high-altitude design with speed and accuracy

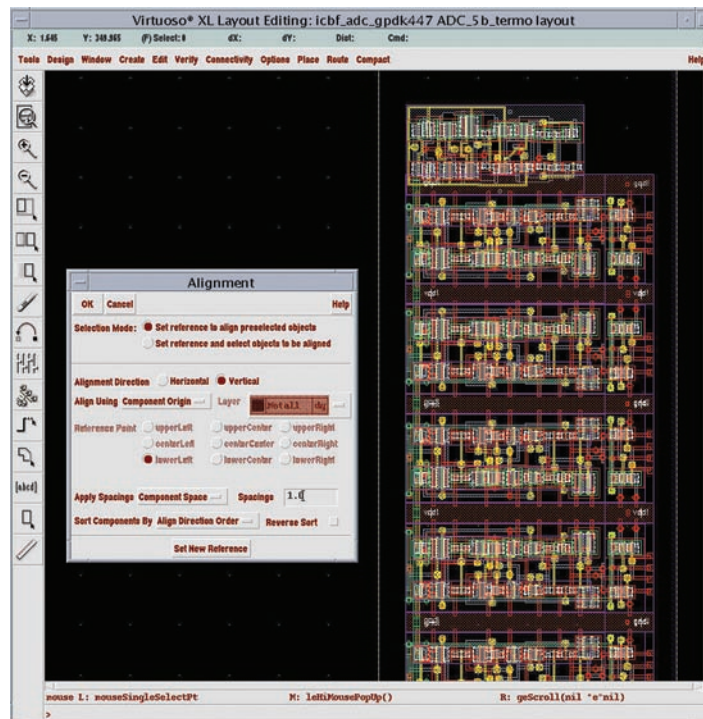


Figure 5: Automated alignment feature provides quick and accurate design-rule-correct placement

## CADENCE SERVICES AND SUPPORT

- Customer-focused solutions that increase ROI, reduce risk, and achieve your design goals faster
  - Collaborative approach and design infrastructure—virtual teaming
  - Proven methodology and flow tuned to your design environment
  - Design and EDA implementation expertise
- Product and flow training to fit your needs and preferred learning style
  - More than 80 instructor-led courses—certified instructors, real-world experience
  - More than 25 Internet Learning Series (iLS) online courses
- Cadence customer support that keeps your design team productive
  - Cadence applications engineers provide technical assistance
  - SourceLink® online support gives you access to software updates, technical documentation, and more—24 hours a day, seven days a week

## FOR MORE INFORMATION

Email us at [info@cadence.com](mailto:info@cadence.com), or log on to [www.cadence.com](http://www.cadence.com)

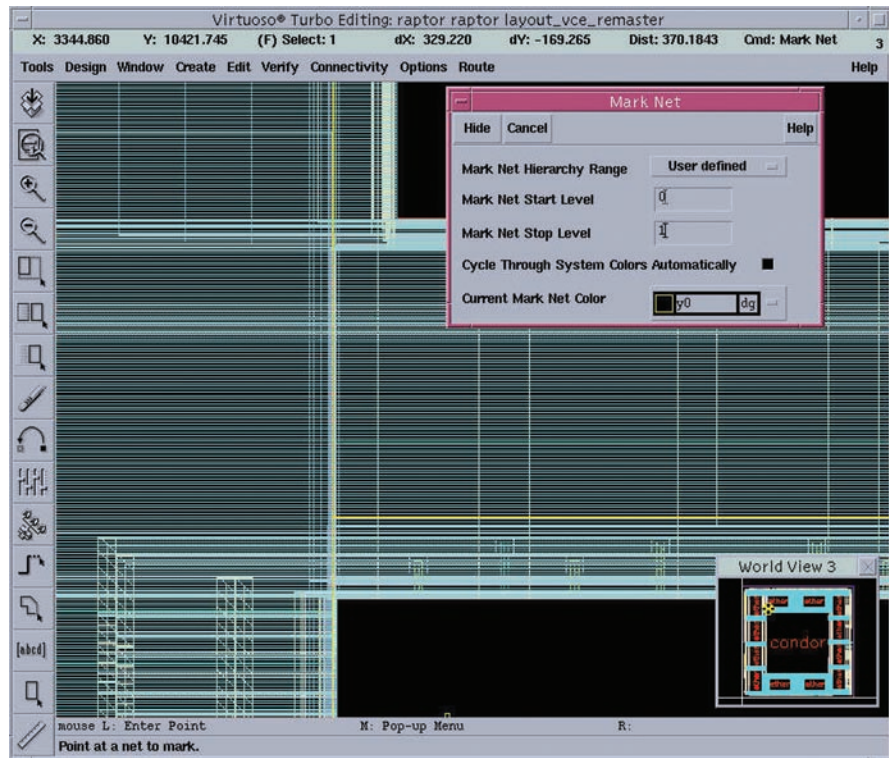


Figure 6: Mark net efficiently traverses the physical design hierarchy and performs continuity checking and highlighting