

## VIRTUOSO AMS DESIGNER SIMULATOR

Cadence® Virtuoso® AMS Designer Simulator is a mixed-signal simulation solution for the design and verification of the largest and most complex mixed-signal SoCs and multichip designs. It is integrated and fully compatible with both the Virtuoso custom design and Incisive™ functional verification platforms.

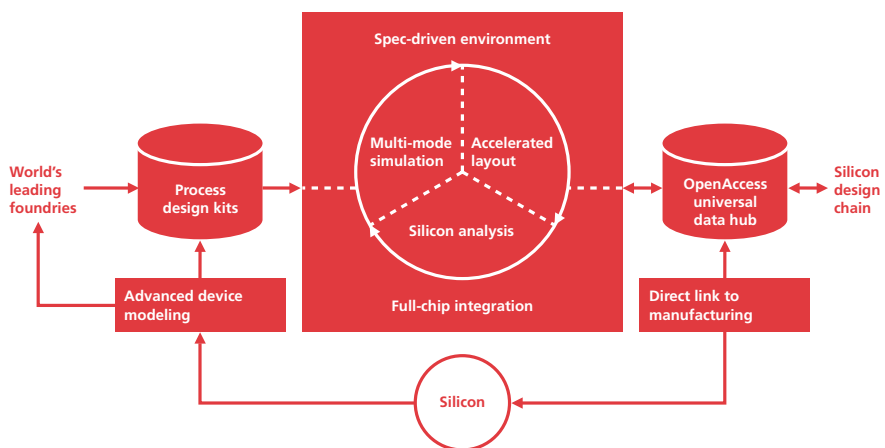


Figure 1: Virtuoso custom design platform

### VIRTUOSO CUSTOM DESIGN PLATFORM

The Virtuoso custom design platform is a comprehensive system for fast, silicon-accurate design and is optimized to support “meet-in-the-middle” design methodologies such as advanced custom design. Virtuoso includes the industry’s only specification-driven environment, multi-mode simulation with common models and equations, vastly accelerated layout, advanced silicon analysis for 0.13 microns and below, and a full-chip, mixed-signal integration environment. The Virtuoso platform is available on the Cadence CDBA database and the industry-standard OpenAccess database. With the Virtuoso platform, design teams can quickly design silicon that is right and on time at process geometries from one micron to 90 nanometers and beyond.

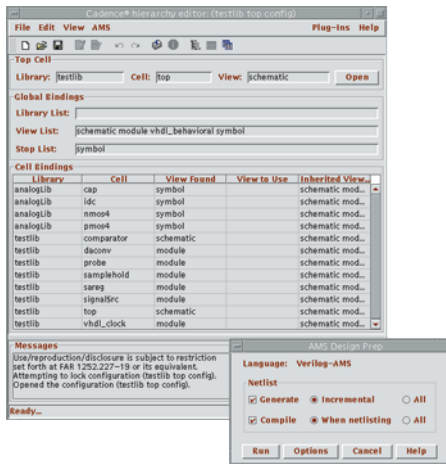


Figure 2: Hierarchy editing and design preparation GUI

## VIRTUOSO AMS DESIGNER SIMULATOR

The Virtuoso AMS Designer Simulator is a single executable language-based mixed-signal simulation solution. With its support of the standard languages, Verilog-AMS and VHDL-AMS, it ensures that mixed-signal SoCs get designed and verified right and on-time, before tapeout. The Virtuoso AMS Designer Simulator is more than just analog and digital simulation — it combines both the analog and the digital design flows together. The AMS environment provides netlisting from schematics and configuration of the design hierarchy and is fully compatible with the Virtuoso custom design platform. The simulation environment and its capability to control the simulation, debug the design, and display the resulting mixed-signal waveforms is fully compatible with the Incisive functional verification platform.

## BENEFITS

- Ensures design quality with proven Virtuoso and Incisive simulation technology
- Supports both top-down and bottom-up design styles for easy adoption
- Quickly detects design failures early in the design phase to make sure the design is ready for tapeout, right on time
- Accelerates simulation with mixed-signal behavioral language support

## FEATURES

### FACILITATES “MEET-IN-THE-MIDDLE” DESIGN METHODOLOGY

The Virtuoso AMS Designer Simulator provides the flexibility to combine IP from different sources and in different formats for today’s SoC designs. It does more than just co-simulate analog and digital blocks. By treating Virtuoso Schematic Editor blocks and textual descriptions equally, the Virtuoso AMS Designer Simulator allows different points of data entry. It is multilingual and accepts descriptions in the standard language formats of Verilog-AMS, VHDL-AMS, Verilog-A, Verilog®, and VHDL, as well as various netlist formats like SPICE and Virtuoso Spectre® Circuit Simulator, or any combination of languages. This multilingual approach allows analog bottom-up and digital top-down design methodologies to meet in the middle.

Different levels of abstraction, like Verilog-AMS or VHDL-AMS behavioral models and schematic representation, are easily interchangeable to allow the design to change over time from full-behavioral to full-transistor. The entire design is configured using the hierarchy editor, which facilitates the viewing and design preparation of a complex mixed-signal design (see Figure 2). Automatically inserted interface elements are used to translate signals from one domain to the next, leaving the user free to experiment with different design configurations to easily trade off

simulation speed for simulation accuracy. The Virtuoso AMS Designer Simulator also supports IP encryption using RSA technology, which allows the user to establish both IP reuse and virtual prototyping methodologies.

### INCORPORATES PROVEN VIRTUOSO AND INCISIVE SIMULATION TECHNOLOGY

The Virtuoso AMS Designer Simulator is a single executable mixed-signal simulator based on the proven technology of Virtuoso Spectre Circuit Simulator and the Incisive Unified Simulator engine. The built-in Virtuoso Spectre circuit solver ensures that the user gets golden simulation results with sign-off quality. The analog results match the waveforms of the analog Virtuoso Spectre simulation. The Virtuoso Spectre solver, inside of the Virtuoso AMS Simulator or as a standalone, uses the same model cards and internal model representations as other simulator solutions, and the model characterization technology incorporated with the Virtuoso platform, to ensure silicon-accurate results. In the verification flow the Virtuoso UltraSim solver is used as the built-in analog simulation engine. This enables final verification of the largest mixed-signal SoCs and multichip designs. With the Incisive unified simulation engine inside of the AMS Simulator, the user gets high-performance native Verilog and VHDL simulation without the need for re-qualification of the digital simulator.

## SPECIFICATIONS

### VIRTUOSO ENVIRONMENT

- Direct Verilog-AMS netlisting
- Hierarchy editor AMS plug-in
- Hierarchy editor configuration
- Support for global design variables and global signals
- Inherited connections

### AMS SIMULATOR

- Single executable mixed-signal/mixed-language simulator (see Figure 3)
- Built-in Virtuoso Spectre/Virtuoso UltraSim analog and Incisive digital engines
- GUI, TCL, batch mode
- Save/restart
- Common mixed-signal waveform database

### COMPILATION

- Native compilation technology
- Intelligent incremental compile to reduce compile times
- GUI or command line
- Compilation into common mixed-signal data structure

### ELABORATION

- Incremental elaboration
- Verilog-AMS discipline resolution
- Automatic Verilog-AMS interface element insertion
- Driver receiver segregation
- Bi-directional interface elements
- Dynamic supply sensitive interface elements

### INCISIVE ENVIRONMENT

- Mixed-signal debugger (see Figure 4)
- Breakpoints on time, position, condition
- Debug stepping through behavioral code, analog, and digital
- Source viewer with Verilog-AMS/VHDL-AMS syntax highlighting
- Direct value access in source viewer
- Waveform window
- Register window

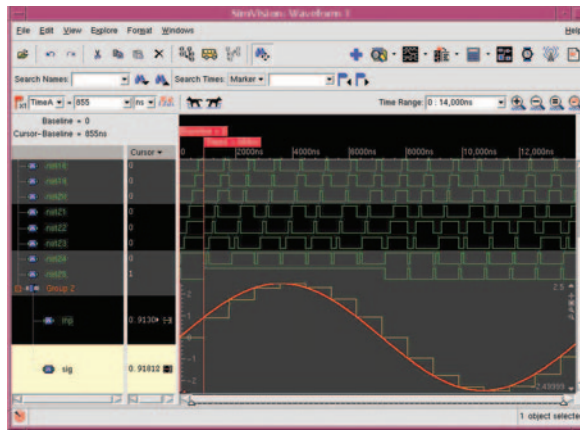


Figure 3: SimVision waveform window for analog and digital analysis

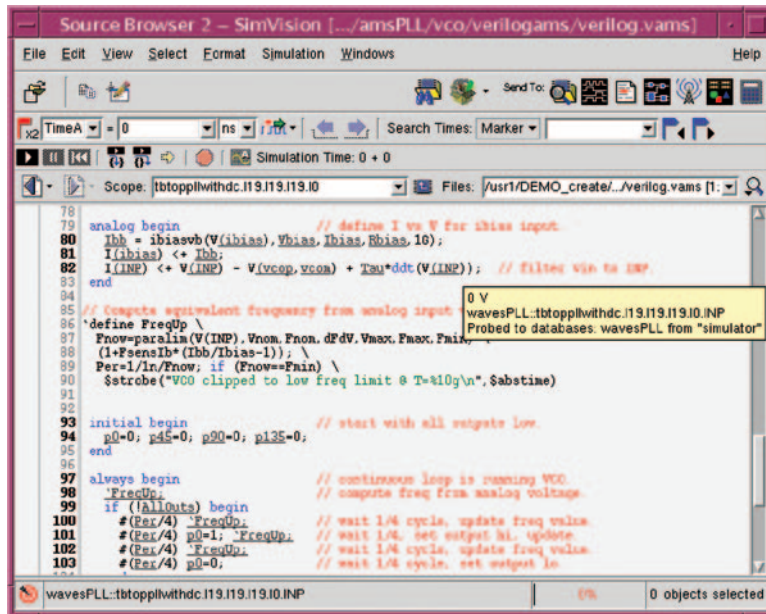


Figure 4: SimVision window for debugging and simulation control

- Calculator
- Schematic tracer
- Signal flow browser
- Error browser
- Digital transaction support

### DESIGN INPUTS

- Cadence CDBA database or OpenAccess database
- Verilog-AMS 2.0
- VHDL-AMS 1076.1
- Verilog (IEEE 1364-1995, majority of IEEE 1364-2001 extensions)
- VHDL (IEEE 1076-1987, IEEE 1076-1993, IEEE 1076.4-2000 (VITAL 2000))

- Spectre, Spice2G6, HSpice netlist formats
- Within Incisive platform: SystemC (OSCI SystemC v2.01), SystemC Verification Library (OSCI SCV 1.0), SystemVerilog

### DESIGN OUTPUTS

- SST2 waveform format analog and digital data
- PSF waveform format for analog data
- Verilog-AMS netlist format

### PLATFORM/OS

- Sun/Solaris
- HP-UX
- Linux

## **CADENCE SERVICES AND SUPPORT**

- Customer-focused solutions that increase ROI, reduce risk, and achieve your design goals faster
  - Collaborative approach and design infrastructure—virtual teaming
  - Proven methodology and flow tuned to your design environment
  - Design and EDA implementation expertise
- Product and flow training to fit your needs and preferred learning style
  - Over 80 instructor-led courses—certified instructors, real-world experience
  - More than 25 Internet Learning Series (iLS) online courses
- Cadence customer support that keeps your design team productive
  - Cadence applications engineers provide technical assistance
  - SourceLink® online support gives you access to software updates, technical documentation, and more—24 hours a day, seven days a week

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