Cost Drivers in Manufacturing of PCBs
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General
PCB fabrication is all about removing the copper you don't want.
Today's design possibilities in the production of printed circuit boards are so diverse and varied that you can barely list them.

In the following presentation: “Cost drivers in manufacturing of PCBs“

I like to indicate and classify the most important PCB features with related process steps and manufacturing methods in the production of PCBs, sorted by their impact on cost.
This attempt, to sort the PCB manufacturing process steps to their cost, sounds simple at first. But it isn’t simple at all because we have to consider:

- Different production strategy
- Different production equipment
- Different technology to create final products
Nevertheless, I’ll give it a try.

The result I like to present today isn’t perfect, but I think it is a good starting point.
Key cost factors in production of Printed Circuit Boards
Cost factors in manufacturing of PCBs

PCB process cost consideration
Cost control must be considered in the early phases of the PCB design process and in some cases even in the actual circuit development.

All additional process steps have an associated cost in terms of process times, materials, consumables, energy and waste treatment.

Process costs impact PCB price regardless of where they are manufactured, and once cost is designed in, it is very hard, if not impossible, to reduce cost without re-design.
Cost factors in manufacturing of PCBs

PCB process cost consideration

Clever design and good engineering are the best solution for board designs with the lowest possible cost index.

Please consider always: important basis fore each PCB design are the IPC Standards: IPC-2220 – IPC2226.
Cost factors in manufacturing of PCBs

PCB process cost consideration

Costing in PCB fabrication is a complex algorithm that account for many variables that have an impact on the overall cost of a part. These variables will weight in the cost by different percentage factors.

Cost is a real factor based on complexity And used materials and equipment, taking into account the efficiency.
The cost factors can be divided into three categories:

- **Cost factors category I**, Significant
- **Cost factors category II**, Important
- **Cost factors category III**, Minor

The allocation to category II and III depends on used equipment and is therefore specific to the manufacturer.
Cost factors in manufacturing of PCBs

Significant cost factors, category I:

- Size of PCB
- Effective utilization of material, Yield
- Layer count
- Complexity of PCB
- Choice of material
Cost factors in manufacturing of PCBs

Size of PCB:

It is trivial:
The larger the PCB, the more it costs.
Cost factors in manufacturing of PCBs

Effective utilization of Material, Yield

Panel utilization is one of the most critical factors with respect to PCB cost.

Good Utilization

Bad Utilization
Utilization of Material, Yield

Manufacturing panels come in many sizes. Some are optimized for special process or materials, others are optimized for volume production with many panel sizes being vendor specific.

Common used Panel sizes:

- 18 X 24” (457 x 610mm)
- 18 X 21” (457 x 533mm)
- 21 X 24” (533 x 610mm)
Cost factors in manufacturing of PCBs

Panel Utilization: Array Considerations

Size:
Panel: 18.0 x 24.0
Array: 5.125 x 10.925
Part: 2.0 x 4.9

Panel Yield:
6 Arrays of 4 Parts
24 Parts Total
77.8% Material Utilization

Matrix:
On Panel: 3 x 2, Origin: X1.2125 Y1.025
On Array: 2 x 2

Spacing:
On Panel: 0.1 x 0.1
On Array: 0.125 x 0.125

Panel Borders:
Left: 1.2125 Right: 1.2125
Top: 1.025 Bottom: 1.025

Array Borders:
Left: 0.5 Right: 0.5
Top: 0.5 Bottom: 0.5

77.8%
= Good utilization!
Cost factors in manufacturing of PCBs

Panel Utilization: Array Considerations

Panel Yield:
- 4 Arrays of 4 Parts
- 16 Parts Total
- 52.8% Material Utilization

Matrix:
- On Panel: 1 x 4, Origin: X3.4375 Y1.6
- On Array: 2 x 2

Spacing:
- On Panel: NA x 0.1
- On Array: 0.125 x 0.125

Panel Borders:
- Left: 3.4375 Right: 3.4375
- Top: 1.6 Bottom: 1.6

Array Borders:
- Left: 0.5 Right: 0.5
- Top: 0.5 Bottom: 0.5

58% = Poor utilization!

Increase cost of 33%
(16 circuits per panel verse
24 circuits per panel)

Source: TTM
Layer count:
Also this cost factor is trivial to understand:
More layers = more production steps
  + more material
  + additional production time.
Layer count:

This cost factor also differs from manufacturer to manufacturer as well.

Change: 1L to 2L: Increase: 35 – 40%
2L to 4L: 30 – 40%
4L to 6L: 30 – 35%
6L to 8L: 30 – 35%
8L to 10L: 20 – 30%
10L to 12L: 20 – 30%
Cost factors in manufacturing of PCBs

Layer count:

Reduction of layer count does not always reduce cost.

If reduction of layer count is achieved by means of more complex technology and/or yields are impacted by aggressive design practices.
Cost factors in manufacturing of PCBs

Cost versus number of layers:

Usually the costs rise is Linear to the number of Layers.

Source: Ronal E. Giachetti
### Complexity of PCB:

<table>
<thead>
<tr>
<th>Technology Change</th>
<th>Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>75/75 μm Linewidth/Space</td>
<td></td>
</tr>
<tr>
<td>Burried Vias drilled 0.2 mm</td>
<td></td>
</tr>
<tr>
<td>Burried V. Annual R. 120 μm</td>
<td></td>
</tr>
<tr>
<td>PTH Via drilled 0.2 mm</td>
<td></td>
</tr>
<tr>
<td>PTH Via Annual Ring 120 μm</td>
<td></td>
</tr>
<tr>
<td>Microvia drilled 0.1 mm</td>
<td></td>
</tr>
<tr>
<td>Microvia Annual Ring 60 μm</td>
<td></td>
</tr>
<tr>
<td>Copper filled PTH Via 20μm</td>
<td></td>
</tr>
<tr>
<td>Thickness of PCB 1.2 mm</td>
<td></td>
</tr>
<tr>
<td><strong>Cost 113%</strong></td>
<td></td>
</tr>
</tbody>
</table>

Before:
- 75/75 μm Linewidth/Space
- Burried Vias drilled 0.3 mm
- Burried V. Annual R. 150 μm
- PTH Via drilled 0.3 mm
- PTH Via Annual Ring 150 μm
- Microvia drilled 0.1 mm
- Microvia Annual Ring 75 μm
- Copper filled PTH Via 20 μm
- Thickness of PCB 1.2 mm

Source: AT&S
Cost factors in manufacturing of PCBs

Complexity of PCBs:

Interconnect Size Scaling

- Solderballs (BGA bis WL/CSP) Ø 800-250 µm
  Ref. I. Panchenko, ECTC 2011

- Flip Chip Ø 90-25 µm
  Ref. M. Müller, TU Dresden

- Cu-Pillar Ø 50-20 µm
  Ref. L. Smith et al., CSR Amkor Technology Inc.

- SLID Cu-Cu Direkt Ø 25-7 µm
  Ref. I. Panchenko et al., Microelectron. Eng., Vol. 117

- Nanointerconnects Ø Nanowire 10-100 nm

Source: Fraunhofer
Micro Via Structures:
Micro Via Structures can also have a big impact on the manufacturing process, since they directly affect the number of lamination cycles. The more variations you have of which layers micro-via start and stop on, the more lamination and drilling steps are needed in the PCB manufacturing process. Which layers the micro via starts and stops on creates a sub-construction, and each sub-construction will require an extra lamination and drilling cycle. (The lamination process is defined as pressing a set of copper layers with dielectrics in between two adjacent copper layers under heat and pressure to form a multilayer PCB laminate).
Cost factors in manufacturing of PCBs

Micro Via Structures:

Cost Optimization:

HDI design reduces overall cost by decreasing the number of layers and size as compared to a STANDARD TECHNOLOGY PCB design for the same level of complexity.

Not only HDI design make the PCBs smaller, lighter, and thinner; but HDI PCBs provide a much superior electrical performance.
Cost factors in manufacturing of PCBs

1x pressed
100%
1 + 6 + 1
Microvias 1 – 2; 1 – 3; 8 – 6; 8 – 7;
Staggered Vias

2x pressed
115%
2 + 4 + 2
Microvias 1 – 2; 8 – 7;
Buried Via 2 – 7;

120%
2 + 4 + 2
Microvias 1 – 2; 2 – 3;
7 – 6; 8 – 7;
Staggered Vias

140%
1 + 6b + 1
Staggered Microvias 1 – 2; 2 – 3;
7 – 6; 8 – 7;
Buried Via 2 – 7;

150%
2 + 4(6b) + 2
Staggered Microvias 1 – 2; 2 – 3;
7 – 6; 8 – 7;
+
Buried Via 3 – 6;

3x pressed
175%
2 + 4b + 2

Source: Fineline
Cost factors in manufacturing of PCBs

Common material selection criteria's:

- Lead free solder compatible (thermal reliability)
- TG (temperature related reliability)
- TCT, CTEz (temperature cycle reliability)
- Degradation Temperature (thermal reliability)
- High thermal conductivity (heat transfer)
- T260, T288 (time to delamination)
- $\varepsilon_r$ (Dk), Df (electrical signal performance)
- CAF resistant
- Mechanical properties (Drop Test, stiffness, etc.)
- Halogen reduced (environmental features)
- etc.
Choice of Material:

The higher the frequency the more important is the choice of materials.

- **Very Low DK**
  - Materials: PTFE (Teflon), LCP
  - Df < 0.003
  - Dk 2.0-3.0
  - Frequency: 35-90 GHz
  - Speed: ~12-30 GB/s

- **Low DK**
  - Materials: Special Resin & Glass clothes
  - Df 0.003-.005
  - Dk 3.0-3.9
  - Frequency: < 30 GHz
  - Speed: ~10 GB/s

- **Enhanced DK**
  - Materials: Special Resin & Glass clothes
  - Df 0.005-.015
  - Dk ~4
  - Frequency: < 20 GHz
  - Speed: ~7 GB/s

- **Standard FR4**
  - Materials: Special Resin & Glass clothes
  - Df > 0.015
  - Dk > 4
  - Frequency: < 5 GHz
  - Speed: ~1.5 GB/s

Source: AT&S
## Cost factors in manufacturing of PCBs

### Choice of Material:

<table>
<thead>
<tr>
<th>Material Group</th>
<th>e.g. Manufacturer/Type</th>
<th>Cost Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Phenolic FR4</td>
<td>ITEQ 180A</td>
<td>1</td>
</tr>
<tr>
<td>High Speed / Mid Low Loss</td>
<td>ITEQ 200LK</td>
<td>1.2</td>
</tr>
<tr>
<td>High Speed / Mid Low Loss</td>
<td>Nelco 4000-13 EP</td>
<td>1.3</td>
</tr>
<tr>
<td>High Speed / Low Loss</td>
<td>Nelco 4000-13 EPSI</td>
<td>3</td>
</tr>
<tr>
<td>High Speed / Low Loss</td>
<td>ITEQ 968</td>
<td>3.5</td>
</tr>
<tr>
<td>High Speed / Low Loss</td>
<td>Panasonic Megtron 6</td>
<td>4</td>
</tr>
<tr>
<td>Polyimide</td>
<td>Nelco N7000-2</td>
<td>3</td>
</tr>
<tr>
<td>High Frequency</td>
<td>Arlon 25N</td>
<td>4</td>
</tr>
<tr>
<td>High Frequency</td>
<td>Rogers 4350B, RO4003</td>
<td>5</td>
</tr>
<tr>
<td>BT Packaging Substrate</td>
<td>Nelco N5000-32</td>
<td>3</td>
</tr>
<tr>
<td>PTFE Based Microwave Materials</td>
<td>Rogers 3000, 5000, 6000</td>
<td>10 - 50</td>
</tr>
</tbody>
</table>

Source: Fineline
Cost factors in manufacturing of PCBs

Note:

Due to the fact that the cost for:
Category II in yellow and Category III in blue will vary greatly depending on involved manufacturer, I did not specified corresponding cost factors in contrast, what I did for Category I in black, PCB features.
Important cost factors, category II:

- Line geometry, track and gap
- Controlled Impedances
- Hole sizes and count of holes
- Plugged, filled Vias copper covered
- Thickness of Copper
- Use of Gold and thickness of Gold
- Tight Tolerances
The differences of the interconnect geometry is significant. The cost as well!
Cost factors in manufacturing of PCBs

Track and gap:

Decreasing Channel Density  Technology Shift  Increasing $

<table>
<thead>
<tr>
<th>Track Width</th>
<th>1.27 mm</th>
<th>1.0 mm</th>
<th>0.8 mm</th>
<th>0.5 mm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drill dia.</td>
<td>12 mils</td>
<td>10 mils</td>
<td>8 mils</td>
<td>6 mils</td>
</tr>
<tr>
<td>Pad dia.</td>
<td>25 mils</td>
<td>20 mils</td>
<td>18 mils</td>
<td>16 mils</td>
</tr>
<tr>
<td>Line width</td>
<td>5 mils</td>
<td>3.5 mils</td>
<td>3.5 mils</td>
<td>N/A</td>
</tr>
<tr>
<td>Max Thk. *</td>
<td>125 mils</td>
<td>100 mils</td>
<td>62 mils</td>
<td>32 mils</td>
</tr>
<tr>
<td>Hole density</td>
<td>400/in.</td>
<td>625/in.</td>
<td>1008/in.</td>
<td>2580/in.</td>
</tr>
<tr>
<td>Channel</td>
<td>40 in./in.^2</td>
<td>50 in./in.^2</td>
<td>31 in./in.^2</td>
<td>Escape Only!</td>
</tr>
</tbody>
</table>

Standard Production

* Hole barrel reliability with lead free assembly

Board thickness limited by drill flute length

Source: TTM
Controlled Impedances:
When the impedance of traces must be controlled, additional costs arise through additional process steps and additional space requirements for the test coupon.
Cost factors in manufacturing of PCBs

Hole sizes and count of holes:

A simple formula:

The more drill holes and the smaller the holes the more expensive.

Size comparison:

- Drill bit with 0.3mm = 300µm diameter
- A human hair, in average 70µm = 2.7mil
- 50µm Microvia
Hole sizes and count of holes:

Aggressive hole size and drill size, along with non standard trace width and air gap can increase price of standard thru hole technology compared to the cost of more simple HDI Technologies.

Small hole size and thick PCB (high Aspect Ratio) increases drilling time and the drill erosion which results in higher cost.
Hole sizes and count of holes:

Pay close attention to aspect ratio and hole size. Often too small of a hole will cause voiding in the filling material. Too large of a hole diameter will cause a larger dimple on the surface of the pad from the filling process.
Hole sizes and count of holes:

The dielectric thickness for any blind hole will need to be reduced to an aspect ratio of 0.8:1.

This will ensure that plating will be able to migrate to the base of the hole to provide acceptable copper thickness.
Cost factors in manufacturing of PCBs

Plugged, filled Vias copper covered:

Source: Peters
Cost factors in manufacturing of PCBs

Thickness of copper:
Cost factors in manufacturing of PCBs

Top 20: Worldwide Copper Mining

- Chile
- China
- United States
- Peru
- Australia
- Congo, D.R.
- Russian Fed.
- Zambia
- Canada
- Mexico
- Kazakhstan
- Poland
- Indonesia
- Brazil
- Mongolia
- Iran
- Laos
- Scandinavia
- Turkey
- Bulgaria

Quelle: ICA
Cost factors in manufacturing of PCBs

Thickness of Copper

Source: Elmatica
Cost factors in manufacturing of PCBs

Thickness of copper:

![Copper foil price index chart]

- Thickness options: 35µm, 70µm, 105µm, 140µm
- Price index ranges from 0 to 3
- Layers: 2 Layer, 4 Layer, 6 Layer, 8 Layer, 10 Layer, 12 Layer

FINELINE
EXCELLENCE IN PCB
Cost factors in manufacturing of PCBs

Thickness of gold

Gold Price-Chart Since year 2000.

Price per troy ounce In US-Dollar.

1 Troy ounce = 31,103 gram
Cost factors in manufacturing of PCBs

**Tight Tolerances**

<table>
<thead>
<tr>
<th>Length tolerance x, y [mm]</th>
<th>Position to track pattern</th>
<th>Position to hole</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Routing</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>±0.15</td>
<td>±0.10</td>
<td>±0.10</td>
</tr>
<tr>
<td>±0.15</td>
<td>±0.10</td>
<td>±0.10</td>
</tr>
<tr>
<td>±0.15</td>
<td>±0.10</td>
<td>±0.10</td>
</tr>
<tr>
<td>60-200</td>
<td></td>
<td></td>
</tr>
<tr>
<td>±0.15</td>
<td>±0.10</td>
<td>±0.10</td>
</tr>
<tr>
<td>±0.15</td>
<td>±0.10</td>
<td>±0.10</td>
</tr>
<tr>
<td>±0.15</td>
<td>±0.10</td>
<td>±0.10</td>
</tr>
<tr>
<td>200-600</td>
<td></td>
<td></td>
</tr>
<tr>
<td>±0.15</td>
<td>±0.10</td>
<td>±0.10</td>
</tr>
<tr>
<td>±0.15</td>
<td>±0.10</td>
<td>±0.10</td>
</tr>
<tr>
<td>±0.15</td>
<td>±0.10</td>
<td>±0.10</td>
</tr>
<tr>
<td>600-2000</td>
<td></td>
<td></td>
</tr>
<tr>
<td>±0.15</td>
<td>±0.10</td>
<td>±0.10</td>
</tr>
<tr>
<td>±0.15</td>
<td>±0.10</td>
<td>±0.10</td>
</tr>
<tr>
<td>±0.15</td>
<td>±0.10</td>
<td>±0.10</td>
</tr>
</tbody>
</table>

The variance between manufacturers, in case of tight tolerances, is big as well. Each deviation from standard caused costs. Main issue is used equipment.
Cost factors in manufacturing of PCBs

- Minor Cost factors category III:
  - Different surface treatments
  - Thickness of PCB
  - Contour of the printed circuit board
  - Solder Mask
  - Legend Print
  - Performance Class: IPC Class II/III etc.
  - Side Plating (Edge Plating)
Cost factors in manufacturing of PCBs

Cost for different surface treatments:

Cost based on a 2 Layer PTH PCB with Format 160 mm x 100 mm, 1.55 mm / 18 µm Copper

Source: AT&S
Cost factors in manufacturing of PCBs

Cost for different surface treatments:

<table>
<thead>
<tr>
<th>Type</th>
<th>Planarity</th>
<th>Solderability</th>
<th>Al Wire Bondable</th>
<th>Au Wire Bondable</th>
<th>Contact Surface</th>
<th>Relative Cost Adder *</th>
</tr>
</thead>
<tbody>
<tr>
<td>HASL</td>
<td>POOR</td>
<td>GOOD</td>
<td>NO</td>
<td>NO</td>
<td>NO</td>
<td>1.0</td>
</tr>
<tr>
<td>LFHASL</td>
<td>FAIR</td>
<td>GOOD</td>
<td>NO</td>
<td>NO</td>
<td>NO</td>
<td>1.0</td>
</tr>
<tr>
<td>OSP</td>
<td>GOOD</td>
<td>GOOD</td>
<td>NO</td>
<td>NO</td>
<td>NO</td>
<td>1.0</td>
</tr>
<tr>
<td>IMM Ag</td>
<td>GOOD</td>
<td>GOOD</td>
<td>YES</td>
<td>NO</td>
<td>NO</td>
<td>1.1</td>
</tr>
<tr>
<td>IMM Sn</td>
<td>GOOD</td>
<td>GOOD</td>
<td>NO</td>
<td>NO</td>
<td>NO</td>
<td>1.1</td>
</tr>
<tr>
<td>ENIG</td>
<td>GOOD</td>
<td>GOOD</td>
<td>YES</td>
<td>NO</td>
<td>YES</td>
<td>1.1</td>
</tr>
<tr>
<td>ENEPIG</td>
<td>GOOD</td>
<td>GOOD</td>
<td>YES</td>
<td>YES</td>
<td>YES</td>
<td>2.5</td>
</tr>
<tr>
<td>Elec Au</td>
<td>GOOD</td>
<td>GOOD</td>
<td>YES (soft only)</td>
<td>YES</td>
<td>YES</td>
<td>3.5</td>
</tr>
</tbody>
</table>

Source: TTM
Cost factors in manufacturing of PCBs

Cost for different surface treatments:

Note:
Please consider the shelf live time of each finish beside all other technical features.

<table>
<thead>
<tr>
<th>Finish:</th>
<th>HASL</th>
<th>Immersion Au (ENIG)</th>
<th>Immersion Ag</th>
<th>Immersion Sn</th>
<th>Organic OSP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shelf live time: [month]</td>
<td>12</td>
<td>12</td>
<td>2.5 - 3</td>
<td>1.5 - 2.5</td>
<td>2 - 3</td>
</tr>
</tbody>
</table>
Cost factors in manufacturing of PCBs

Cost for different surface treatments

1 Layer PCB, HAL Finish

Material: 60.0%
Drill & Rout: 20.0%
Surface: 10.0%
Layout: 5.0%
Soldermask: 3.0%
Electrical Test: 3.0%
Inspection: 2.0%

4 Layer PCB, HAL Finish

Material: 25.0%
Plating: 20.0%
Layout: 15.0%
Drill & Rout: 10.0%
Soldermask: 10.0%
Lamination: 5.0%
Inner Layers: 5.0%
Inspection: 5.0%
Electrical: 5.0%
Surface: 5.0%

Source: AT&S
Cost factors in manufacturing of PCBs

Thickmess of PCB:

The standard thickness for PCBs is:

1.6mm (0.063 ").

It depends on the manufacturers whether thinner PCBs $\geq 0.8$ mm will have same, lower or even higher price levels. Thicker versions are becoming increasingly expensive. Attention! Always note the "Aspect Ratio".
Cost factors in manufacturing of PCBs

Contour of the printed circuit board:

Large price fluctuations between different suppliers are possible. Significant price fluctuations in case z-axes routing is required.
Solder Mask:

Significant additional costs only in case of Advanced clearance and thickness requirements.

Source: Fineline
Cost factors in manufacturing of PCBs

Legend Print:

Nothing to write home about 😊
Cost factors in manufacturing of PCBs

Performance class: IPC Class II/III etc.

The technical differences between classes 2 and 3 are rather small. From 105 features, described in IPC-6012B, only 12 features differ between Class II and Class III.

The higher cost for PCBs manufactured in compliance with class III requirement results from the higher testing effort only involved.
Side-Plating (Edge-Plating):
It is possible to metallize the edges of the PCB to increase the EMC strength and reduce the emission of the PCBA as well.

Further example: The plug has a metallic separation surface located in the middle area of this connector. The PCB side is partial metallized to serve as a reference plane.
3 Cost index of major process operations for HDI PCBs
Cost Index for a 12 Layer HDI PCB

For the most accurate cost estimate, Fineline recommends taking an existing design scope and then adjusting the requirements based on estimated technologies required. These estimates will provide more relative data points to make any cost per technology decision, and prevent surprises later in the process when resources have been committed to a design.
HDI process cost index consideration:

For the purpose of developing a basic cost index for engineering purposes, one way to look at the fabrication process is to keep track of the number of major operations.

Following, I defined 7 costly processing steps for determining a HDI base cost index.
Cost Index for a 12 Layer HDI PCB

- Inner Layer processing
- Copper Plating processing
- High Pressure Lamination
- Mechanical Drilling
- Laser Drilling
- Vias covered with copper
- Vias filled with copper

7 costly processing steps for determining a HDI base cost index
HDI Cost Index Consideration:

The following examples use a 12 layer printed circuit to illustrate how different via configurations impact manufacturing complexity.

Starting with a standard through hole design, than adding blind and buried vias, micovias and via-In-Pad technologies.
Cost Index for a 12 Layer HDI PCB

12 Layer PCB with Through Hole Vias

Quelle: TTM / Fineline
Cost Index for a 12 Layer HDI PCB

<table>
<thead>
<tr>
<th>Process</th>
<th>Cost Index</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inner Layer Processing</td>
<td>5</td>
</tr>
<tr>
<td>Copper Plating Processing</td>
<td>1</td>
</tr>
<tr>
<td>High Pressure Lamination</td>
<td>1</td>
</tr>
<tr>
<td>Mechanical Drilling</td>
<td>1</td>
</tr>
<tr>
<td>Laser Drilling</td>
<td>0</td>
</tr>
<tr>
<td>Via covered by copper</td>
<td>0</td>
</tr>
<tr>
<td>Vias copper filled</td>
<td>0</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>8</strong></td>
</tr>
</tbody>
</table>

Cost Index = 8

<table>
<thead>
<tr>
<th>Process</th>
<th>Cost Index</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inner Layer Processing</td>
<td>5</td>
</tr>
<tr>
<td>Copper Plating Processing</td>
<td>1</td>
</tr>
<tr>
<td>High Pressure Lamination</td>
<td>1</td>
</tr>
<tr>
<td>Mechanical Drilling</td>
<td>1</td>
</tr>
<tr>
<td>Laser Drilling</td>
<td>1</td>
</tr>
<tr>
<td>Via covered by copper</td>
<td>0</td>
</tr>
<tr>
<td>Vias copper filled</td>
<td>0</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>9</strong></td>
</tr>
</tbody>
</table>

Cost Index = 9

<table>
<thead>
<tr>
<th>Process</th>
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<tbody>
<tr>
<td>Inner Layer Processing</td>
<td>5</td>
</tr>
<tr>
<td>Copper Plating Processing</td>
<td>1</td>
</tr>
<tr>
<td>High Pressure Lamination</td>
<td>1</td>
</tr>
<tr>
<td>Mechanical Drilling</td>
<td>1</td>
</tr>
<tr>
<td>Laser Drilling</td>
<td>2</td>
</tr>
<tr>
<td>Via covered by copper</td>
<td>0</td>
</tr>
<tr>
<td>Vias copper filled</td>
<td>0</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>10</strong></td>
</tr>
</tbody>
</table>

Cost Index = 10

Quelle: TTM / Fineline
## Cost Index for a 12 Layer HDI PCB

<table>
<thead>
<tr>
<th>Process</th>
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</thead>
<tbody>
<tr>
<td>Inner Layer Processing</td>
<td>4</td>
</tr>
<tr>
<td>Copper Plating Processing</td>
<td>2</td>
</tr>
<tr>
<td>High Pressure Lamination</td>
<td>3</td>
</tr>
<tr>
<td>Mechanical Drilling</td>
<td>2</td>
</tr>
<tr>
<td>Laser Drilling</td>
<td>0</td>
</tr>
<tr>
<td>Via covered by copper</td>
<td>0</td>
</tr>
<tr>
<td>Vias copper filled</td>
<td>0</td>
</tr>
<tr>
<td><strong>Cost Index = 11</strong></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Process</th>
<th>Cost Index</th>
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</thead>
<tbody>
<tr>
<td>Inner Layer Processing</td>
<td>5</td>
</tr>
<tr>
<td>Copper Plating Processing</td>
<td>1</td>
</tr>
<tr>
<td>High Pressure Lamination</td>
<td>1</td>
</tr>
<tr>
<td>Mechanical Drilling</td>
<td>1</td>
</tr>
<tr>
<td>Laser Drilling</td>
<td>2</td>
</tr>
<tr>
<td>Via covered by copper</td>
<td>1</td>
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<tr>
<td>Vias copper filled</td>
<td>1</td>
</tr>
<tr>
<td><strong>Cost Index = 12</strong></td>
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</tr>
</tbody>
</table>

### Fineline Excellence in PCB

Quelle: TTM / Fineline
Cost Index for a 12 Layer HDI PCB

<table>
<thead>
<tr>
<th>Process</th>
<th>Cost Index</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inner Layer Processing</td>
<td>4</td>
</tr>
<tr>
<td>Copper Plating Processing</td>
<td>2</td>
</tr>
<tr>
<td>High Pressure Lamination</td>
<td>3</td>
</tr>
<tr>
<td>Mechanical Drilling</td>
<td>2</td>
</tr>
<tr>
<td>Laser Drilling</td>
<td>2</td>
</tr>
<tr>
<td>Via covered by copper</td>
<td>2</td>
</tr>
<tr>
<td>Vias copper filled</td>
<td>0</td>
</tr>
</tbody>
</table>

Cost Index = 13

<table>
<thead>
<tr>
<th>Process</th>
<th>Cost Index</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inner Layer Processing</td>
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</tr>
<tr>
<td>Copper Plating Processing</td>
<td>2</td>
</tr>
<tr>
<td>High Pressure Lamination</td>
<td>2</td>
</tr>
<tr>
<td>Mechanical Drilling</td>
<td>1</td>
</tr>
<tr>
<td>Laser Drilling</td>
<td>4</td>
</tr>
<tr>
<td>Via covered by copper</td>
<td>0</td>
</tr>
<tr>
<td>Vias copper filled</td>
<td>0</td>
</tr>
</tbody>
</table>

Cost Index = 13

Quelle: TTM / Fineline
## Cost Index for a 12 Layer HDI PCB

<table>
<thead>
<tr>
<th>Process</th>
<th>Cost Index</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inner Layer Processing</td>
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<td>4</td>
</tr>
<tr>
<td>High Pressure Lamination</td>
<td>4</td>
</tr>
<tr>
<td>Mechanical Drilling</td>
<td>4</td>
</tr>
<tr>
<td>Laser Drilling</td>
<td>0</td>
</tr>
<tr>
<td>Via covered by copper</td>
<td>0</td>
</tr>
<tr>
<td>Vias copper filled</td>
<td>0</td>
</tr>
</tbody>
</table>

**Cost Index = 15**

<table>
<thead>
<tr>
<th>Process</th>
<th>Cost Index</th>
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</thead>
<tbody>
<tr>
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<tr>
<td>Copper Plating Processing</td>
<td>2</td>
</tr>
<tr>
<td>High Pressure Lamination</td>
<td>2</td>
</tr>
<tr>
<td>Mechanical Drilling</td>
<td>1</td>
</tr>
<tr>
<td>Laser Drilling</td>
<td>4</td>
</tr>
<tr>
<td>Via covered by copper</td>
<td>2</td>
</tr>
<tr>
<td>Vias copper filled</td>
<td>2</td>
</tr>
</tbody>
</table>

**Cost Index = 17**

<table>
<thead>
<tr>
<th>Process</th>
<th>Cost Index</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inner Layer Processing</td>
<td>4</td>
</tr>
<tr>
<td>Copper Plating Processing</td>
<td>2</td>
</tr>
<tr>
<td>High Pressure Lamination</td>
<td>2</td>
</tr>
<tr>
<td>Mechanical Drilling</td>
<td>4</td>
</tr>
<tr>
<td>Laser Drilling</td>
<td>2</td>
</tr>
<tr>
<td>Via covered by copper</td>
<td>2</td>
</tr>
<tr>
<td>Vias copper filled</td>
<td>2</td>
</tr>
</tbody>
</table>

**Cost Index = 18**

---

**Quelle: TTM / Fineline**
## Cost Index for a 12 Layer HDI PCB

<table>
<thead>
<tr>
<th>Process</th>
<th>Cost Index</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inner Layer Processing</td>
<td>3</td>
</tr>
<tr>
<td>Copper Plating Processing</td>
<td>3</td>
</tr>
<tr>
<td>High Pressure Lamination</td>
<td>3</td>
</tr>
<tr>
<td>Mechanical Drilling</td>
<td>2</td>
</tr>
<tr>
<td>Laser Drilling</td>
<td>4</td>
</tr>
<tr>
<td>Via covered by copper</td>
<td>2</td>
</tr>
<tr>
<td>Vias copper filled</td>
<td>2</td>
</tr>
<tr>
<td><strong>Cost Index = 19</strong></td>
<td></td>
</tr>
</tbody>
</table>

**Quelle: TTM / Fineline**
Miscellaneous and closing remarks
As I mentioned already:

For the most accurate cost estimate, Fineline recommends taking an existing design scope and then adjusting the requirements based on estimated technologies required. These estimates will provide a more relative data points to make any cost per technology decision, and prevent surprises later in the process when resources have been committed to a design.
Cost factors in manufacturing of PCBs

1x pressed
- 100%
- 1 + 6 + 1
- Microvias 1 – 2; 1 – 3; 8 – 6; 8 – 7;
- Staggered Vias

2x pressed
- 115%
- 2 + 4 + 2
- Microvias 1 – 2; 8 – 7;
- Buried Via 2 – 7;

- 120%
- 2 + 4 + 2
- Microvias 1 – 2; 2 – 3; 7 – 6; 8 – 7;
- Staggered Vias

- 140%
- 1 + 6b + 1
- Staggered Microvias 1 – 2; 2 – 3; 7 – 6; 8 – 7;
- Buried Via 2 – 7;

3x pressed
- 150%
- 2 + 4(6b) + 2

- 175%
- 2 + 4b + 2
- Staggered Microvias 1 – 2; 2 – 3; 3 – 6;
- Buried Via 3 – 6;

Source: Fineline
Sanmina PCB Fabrication – Cost Ratio Calculator

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Initial</th>
<th>New</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>Layers</td>
<td>6</td>
<td>6</td>
<td>1.00</td>
</tr>
<tr>
<td>Material</td>
<td>FR-4 Std Tg</td>
<td>FR-4 Std Tg</td>
<td>1.00</td>
</tr>
<tr>
<td>Thickness</td>
<td>50-70 mils</td>
<td>50-70 mils</td>
<td>1.00</td>
</tr>
<tr>
<td>Drilled Hole Size</td>
<td>13.5 mils</td>
<td>13.5 mils</td>
<td>1.00</td>
</tr>
<tr>
<td>Impedance</td>
<td>15%</td>
<td>15%</td>
<td>1.00</td>
</tr>
<tr>
<td>Copper Thickness</td>
<td>0.5-1 oz</td>
<td>0.5-1 oz</td>
<td>1.00</td>
</tr>
<tr>
<td>Blind Via</td>
<td>None</td>
<td>None</td>
<td>1.00</td>
</tr>
<tr>
<td>Buried Via</td>
<td>None</td>
<td>None</td>
<td>1.00</td>
</tr>
<tr>
<td>BC™ Cores (2mil)</td>
<td>None</td>
<td>None</td>
<td>1.00</td>
</tr>
<tr>
<td>Inner Layer Line Width/Space</td>
<td>5/5 mil</td>
<td>5/5 mil</td>
<td>1.00</td>
</tr>
<tr>
<td>Outer Layer Line Width/Space</td>
<td>5/5 mil</td>
<td>5/5 mil</td>
<td>1.00</td>
</tr>
</tbody>
</table>

Sanmina PCB Fabrication – Cost Ratio Calculator


Instead of 6 Layer New: 10 Layer
Cost Ratio Change from: “1” to “1.56”

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Initial</th>
<th>New</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>Layers</td>
<td>6</td>
<td>10</td>
<td>1.56</td>
</tr>
<tr>
<td>Material</td>
<td>FR-4 Std Tg</td>
<td>FR-4 Std Tg</td>
<td>1.00</td>
</tr>
<tr>
<td>Thickness</td>
<td>50-70 mils</td>
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<td>1.00</td>
</tr>
<tr>
<td>Drilled Hole Size</td>
<td>13.5 mils</td>
<td>13.5 mils</td>
<td>1.00</td>
</tr>
<tr>
<td>Impedance</td>
<td>15%</td>
<td>15%</td>
<td>1.00</td>
</tr>
<tr>
<td>Copper Thickness</td>
<td>0.5-1 oz</td>
<td>0.5-1 oz</td>
<td>1.00</td>
</tr>
<tr>
<td>Blind Via</td>
<td>None</td>
<td>None</td>
<td>1.00</td>
</tr>
<tr>
<td>Buried Via</td>
<td>None</td>
<td>None</td>
<td>1.00</td>
</tr>
<tr>
<td>BC™ Cores (2mil)</td>
<td>None</td>
<td>None</td>
<td>1.00</td>
</tr>
<tr>
<td>Inner Layer Line Width/Space</td>
<td>5/5 mil</td>
<td>5/5 mil</td>
<td>1.00</td>
</tr>
<tr>
<td>Outer Layer Line Width/Space</td>
<td>5/5 mil</td>
<td>5/5 mil</td>
<td>1.00</td>
</tr>
</tbody>
</table>
Closing Remark

Cost control must be already considered in the early phase of PCB design.

Each process step create associated cost in terms of process times, materials, energy and waste treatment.

Each PCB designer should know and understand the basics how to manufacture a PCB.

Smart design and good engineering are always the best solution for PCB design with lowest possible cost index.
It's unwise to pay too much, but it's worse to pay too little.

“It's unwise to pay too much, but it's worse to pay too little. When you pay too much, you lose a little money - that's all. When you pay too little, you sometimes lose everything, because the thing you bought was incapable of doing the thing it was bought to do. The common law of business balance prohibits paying a little and getting a lot - it can't be done.

If you deal with the lowest bidder, it is well to add something for the risk you run, and if you do that you will have enough to pay for something better.”

John Ruskin (1819-1900)
THANK'S FOR LISTENING