Simultaneous Switching Noise (SSN)
A Power Integrity Issue

Design with decaps intentionally removed to demonstrate how poor PI performance dramatically affects SI performance.

Non-ideal PDN
Power-aware SI simulation
significant SSN effect

Ideal PDN
classical SI simulation
minimal SSN effect

Graphs showing voltage over time for non-ideal and ideal PDNs.
Differences in S-parameters for ideal vs. actual return paths

Capturing complex EM interaction in 3D structure is absolutely necessary
Components require precise control of temperature at each via/ball/pin

- Electrical / thermal co-design is the only way to meet such requirement.

- IPC guidelines provide a manual procedure to estimate localized temperature but using such a crude method can lead to un-safe or costly designs.

4.3 Socket Maximum Temperature

The power dissipated within the socket is a function of the current at the pin level and the effective pin resistance. To ensure socket long term reliability, Intel defines socket maximum temperature using a via on the underside of the motherboard. Exceeding the temperature guidance may result in socket body deformation, or increases in thermal and electrical resistance which can cause a thermal runaway and eventual electrical failure. The guidance for socket maximum temperature is listed below:

- Via temperature under socket < 96 °C

Note:

Based on the system enabling boundary condition, the solder ball temperature can vary and needs to be comprehended for reliability assessment.
Power Integrity vs. Power-Aware SI

PI and SI comprise “Power-Aware SI” but …

- PI is unique from SI
  - DC requirements are critical and not part of SI
  - Best to consider PI early in design flow
    - Stack-up definition must consider both DC and AC requirements
    - PDN cap selection must be reflected in BOM and schematic
    - Decap placement best performed pre-route
  - Post-layout verification of PI
    - Changes made during physical design implementation often impact PI performance for impedance and emissions

- PI and SI together are too complex to not be first considered individually
Power Integrity Design Tasks

- **Feasibility studies and noise budgets for the PDN**
  - Driving stack-up requirements

- **DC / low frequency**
  - VRM selection and implementation
    - bulk cap selection
  - IR Drop
  - Current Constraints (both planes and vias)
  - Sense line placement
  - Thermal verification

- **AC / high frequency**
  - Decap (and EMIcap) selection
  - Cap placement
  - Impedance and/or noise requirement checking
  - PDN model extraction for subsequent simulation
  - Emissions verification
Sigrity Products Overview

- **Power Integrity**
  - PowerDC
  - PowerSI
  - OptimizePI

- **Power Aware SI**
  - SPEED2000
  - SystemSI
  - Broadband SPICE
  - T2B
  - PowerSI 3D-FEM

- **Package Design/Assesment**
  - UPD
  - XtractIM

- **CO-design / Co-analysis**
  - OrbitIO
  - XcitePI
PowerDC is an efficient DC sign-off solution for IC package and PCB designs with electrical / thermal co-simulation to maximize accuracy. IR drop and current hot-spots are quickly pinpointed. Best remote sense locations are automatically found.
PowerDC
Electrical, Thermal and Co-simulation

1. Table based IR Drop and Current Constraint results

<table>
<thead>
<tr>
<th>Sink Name</th>
<th>Model</th>
<th>Nominal Voltage (V)</th>
<th>Input Tolerance (%)</th>
<th>Actual Voltage (V)</th>
<th>Margin (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SINK_U2+33V_GND</td>
<td>Equal Current</td>
<td>3.3</td>
<td>2</td>
<td>3.22433</td>
<td>-0.00916</td>
</tr>
<tr>
<td>SINK_U1+33V_GND</td>
<td>Equal Current</td>
<td>3.3</td>
<td>2</td>
<td>3.21606</td>
<td>-0.0179395</td>
</tr>
<tr>
<td>SINK_U2flash2+33V_GND</td>
<td>Equal Current</td>
<td>3.3</td>
<td>2</td>
<td>3.26149</td>
<td>0.0274923</td>
</tr>
<tr>
<td>SINK_U2flash1+33V_GND</td>
<td>Equal Current</td>
<td>3.3</td>
<td>2</td>
<td>3.2609</td>
<td>0.0269027</td>
</tr>
<tr>
<td>SINK_U2+1.5V_GND</td>
<td>Equal Current</td>
<td>1.5</td>
<td>1</td>
<td>1.49328</td>
<td>0.00827637</td>
</tr>
</tbody>
</table>

2. Plots of voltage, current, power, temperature, etc.
3. HTML sign-off report
Temperature dependent material (both metal and dielectric) properties significantly affect current flow and temperature distributions.

Analyzing best case (25C) and worst case (80C) uniform ambient temperature distributions provides only a too-broad lower/upper bound and inaccurate IR drop results.

Why you should care!
Power DC
Measurement Correlation

Electro-Thermal
PowerDC Simulation
Measurement

COIL1: 66.5 °C/68.2°C
CS9: 64.4 °C/63.6°C
CS10/CS12: 62.7 °C/63.5°C
L3/CS2: 59.1 °C/59.9°C
Q18-21: 63.8 °C/64.4°C
Q23: 59.5 °C/59.2°C
Q24: 58.9 °C/58.8°C
Q51: 52.8 °C/58.6°C
Q52: 59.1 °C/59.2°C
U9: 67.3 °C/66.5°C
U10: 94.2 °C/96.3°C
U15: 71.9 °C/72.6°C
U19: 62.8 °C/63.1°C
U20: 64.6 °C/61.5°C
PowerDC Distribution Plots

Voltage Distribution Plot

Current Density Plot (current vector)

Power Density Plot

Via Current Plot

Current Density Plot

Power Loss Plot

PowerDC Distribution Plots

Voltage Distribution Plot

Current Density Plot (current vector)

Power Density Plot

Via Current Plot

Current Density Plot

Power Loss Plot
PowerDC
Distribution Plots

Pin IR drop Plot

Pin Resistance Plot

Temperature Plot
PowerDC
SignOff Reports
PowerDC
Primary Advantages

- The first and only integrated and automated electrical and thermal co-simulation for PCBs and packages
- Patented time saving automation for remote sense line positioning
- Fastest and most accurate IR drop solution
- Broad range of visualization options for rapid design improvement
- Unique block diagram results visualization supporting what-if updating
PowerSI is an advanced signal integrity, power integrity and design-stage EMI solution. Supports S-parameter model extraction and provides robust frequency domain simulation for entire IC package and PCB designs.
PowerSI
Virtual Network Analyzer
Extracts N-port Impedance and S-parameters

Figure 1. 4L and 6L FCBGA packages.

Figure 3. Probing the impedance of the power distribution network as seen from the bumps.

Figure 4. Correlation between simulations (dotted line) and measurements (solid line) of the FBVDDQ power distribution network of 4L and 6L packages (a) package alone, and (b) package mounted on the corresponding board.

Power SI
Correlation of Simulated & Measured PDN

- Memory DIMM PCB
- Bare board w/ decaps
- PDN impedance measured

Log Scale

Linear Scale

red = vcc
green = ground
Power SI
Broadband Model PI/SI Extraction

Only pwr/gnd may be extracted or signals may also be included.

Here, the S-parameters are extracted for eight differential pairs, plus their associated pwr/gnd nets, from die-side to BGA-side of a package.
Power SI
Source-free and Driven PDN Resonances are characterized

3D display

2D display

PDN Impedance Profile point-n-click probed at cursor location
Power SI
Near and Far fields through Postprocessing results after analysis

<table>
<thead>
<tr>
<th>Measurements</th>
<th>Hybrid Analysis</th>
</tr>
</thead>
<tbody>
<tr>
<td>-H-Field Distribution</td>
<td>-H-Field Distribution</td>
</tr>
<tr>
<td>-Frequency of Hot Spot</td>
<td>-Frequency of Hot Spot</td>
</tr>
</tbody>
</table>

Far Fields

Near Fields

FCC

Hot Spots
Power SI 3D FEM

PowerSI 3D FEM provides full-wave solver capability inside PowerSI for accurate analysis of complex 3D structures. The software is tailored to IC package and PCB structures. Adaptive meshing assures accuracy combined with fast simulation time.
Power SI 3D FEM Simulation

Example: Package core PDN
- Simulation from the Power SI GUI
- Accuracy comparable to other 3D FEM tools
- Greater low frequency stability
- Significantly faster simulation times

Red = PSI-3DFEM
Blue = 3rd party

Aqua = PSI-3DFEM
Yellow = 3rd party
PowerSI
Primary Advantages

- Market leader and product of choice of companies where power integrity is essential
- Highly accurate modeling of layout structures
- Ability to handle general n-terminal component models
- Unique capability for ensuring accuracy down to DC (patent pending)
- Targeted workflows to streamline operations
- Integration with 3D solution

Frequency domain SI, PI and EMC
Optimize PI is a highly automated board and IC Package AC frequency analysis solution. Supports pre- and post-layout decap studies and identifies impedance issues. Decap implementations are optimized for performance and cost.
Optimize PI
Explore design tradeoffs quickly

- Device/VRM location and mounting layer
- Locations and mounting layers of decaps (top/bottom/under)
- Fanout from decaps
- Stackup and plane separation
- Voids on power and GND plane
Optimize PI
Pre-route and Post-route optimization results for BOM and placement

1\textsuperscript{st} Optimization
Impedance (Ohm)

\begin{itemize}
\item \textbf{39 decaps} \\
\$0.55
\end{itemize}

Optimization Objective:

\textbf{Number of Decaps}

- Setup: 10 minutes
- Simulation: 1 minute
- Decap optimization: 6 minutes
- Total pre-layout analysis time: 17 minutes

2\textsuperscript{nd} Optimization
Impedance (Ohm)

\begin{itemize}
\item \textbf{44 decaps} \\
\$0.42
\end{itemize}

Optimization Objective:

\textbf{Cost}
Optimize PI
Example

**Before**

OptimizePI reduces decoupling capacitor count.

**(before)**

**After**

OptimizePI™ Cost-Based PDS Design

![Graph showing PDS Impedance vs. Decoupling Capacitor Cost](image)

- Lower Cost, Same Performance
- Original Design
- Higher Performance, Same Cost
Optimize PI
Validation of improved performance at lower cost in both time and frequency domain
Optimize PI
Quickly identify ineffective Decap locations with loop inductance analysis
OptimizePI
EMIcap Selection and Placement
Impedance at all PDN locations

Impedance vs. Frequency

Scheme 1
Top

Scheme 2
Top

2 added emicaps (100nF)
AC=1 source at the device

Far E-field vs. frequency

Before
After

Near E-field at 580MHz
same scale for each plot
OptimizePI  
Primary Advantages

- Automated decap optimization and verification features
- Clear presentation of economic benefits from decap optimization
- Flexibility in meeting targeted objectives (performance, cost, area …)
- Easy-to-use AC analysis environment.
- Unique device impedance and EMI resonance checking
- Support for early-stage studies and post-post layout verification

Automated positioning of EMI decaps
SPEED2000 is a comprehensive PCB/package layout based time domain EM simulation tool for signal integrity, power integrity and design-stage EMI analysis. It supports advanced layout checking for design sign-off and debug.
SPEED2000
Primary advantages

- Unique animation of transient field propagation across PCBs and packages
- Exceptional layout based signal integrity simulation including non-ideal power and ground systems
- Only solution for EMC simulation with non-linear drivers and receivers
- Customized workflows for layout electrical performance checks
- Streamlined layout based DDR SSO simulation support
XtractIM is a fast IC package RLC extraction and assessment solution with an option to generate highly accurate broadband models. Supports a broad range of package types including BGA, SiP and leadframe designs.
XtractIM
Primary Advantages

- Built in package assessment rapidly identifies potential package defects
- Unsurpassed extraction speed and ease of use
- Able to address the broadest range of packages (single die & multi-die; flip chip, wirebond & leadframe)
- Users control model extraction precision (RLCG to broadband accurate)
- Easy to learn for occasional users and layout designers
- HTML reports that can be readily shared with partners

Red curve shows impact of Per-pin self loop inductance
“Brocade became an early adopter of Cadence Sigrity’s SystemSI – Parallel Bus Analysis software, which we use to perform rapid DDR3 simulations that accurately incorporate crucial power delivery system impacts to ensure we can meet our tight timing margins.”

Shahriar Mokhatarzad
Brocade
June 1, 2011
SystemSI is a comprehensive and automated signal integrity environment for the accurate assessment of high-speed chip-to-chip system designs. Ensures robust parallel bus and serial link interface implementations.
SystemSI
Primary Advantages

- Fastest, most advanced channel simulation engine
- Simplified model connections with Model Connection Protocol (MCP) and block-wise editor
- Highly automated measurement and reporting capabilities
- Unique AMI IP library for model generation
- Clear linkage between schematic model and physical layout
- Early studies supported with accurate 3D FEM based Via Wizard

Above = DDR / Below = Serial Link
“Traditional IBIS models do not provide the accuracy needed for SSO and transistor modes take so long to run that they are not viable either. With T2B we expect to be able to convert transistor level models to IBIS 5.0 power-aware models that retain the accuracy of the original. This enables us to support a full bus simulation flow to help us quickly make design improvements.”

September 1, 2011
Naoshi Higaki
Fujitsu Semiconductor

Freely available without a license:

- Broadband SPICE
- S-parameter tuning & conversion to SPICE
- Model Connection Protocol (MCP)
- Broadband Network Parameter Format (BNP)

Model conversion and generation utilities
Broadband SPICE offers a combination of S-parameter checking, tuning and extraction capability to convert N-port network parameters to efficient SPICE compatible circuits that can be used in time domain simulations.
Broadband SPICE
Primary Advantages

✓ Market leader for micro-model extraction
✓ Extensive checking functions for S-parameter model tuning and improvement
✓ Automated adaptive port reference impedance technique to enhance model accuracy (patent pending)
✓ Enables faster S-parameter simulations
✓ Integration with PowerSI and SystemSI for streamlined design flows

Red curve shows impact of S-parameter tuning
Transistor to Behavioral Model Conversion (T2B) provides an efficient way to create accurate models for SSO and other simulations. These models run an order of magnitude faster than the original transistor models.
T2B
Primary Advantages

✓ Industry’s most advanced tool for converting transistor models to IBIS
✓ Provides IBIS v5.0 power-aware model support
✓ Cadence Sigrity’s IBIS plus model provides even more accuracy
✓ Convenient GUI verifies conversion accuracy
✓ Makes full bus simulations practical that would take weeks otherwise
✓ Exceptional field support worldwide

Impact of pre-driver current

Built-in simulation check compares transistor to IBIS power-aware model
Model Connection Protocol (MCP) simplifies time consuming model connections to support multi-structure simulations. Tedious and error prone operations are streamlined to make complex simulations practical.
MCP
Primary Advantages

- Open format, available from Cadence Sigrity without charge
- Simplifies connections to enable multi-structure simulations
- Reduces error-prone connection tasks
- Makes it practical to predict localized behavior by enabling per-pin connections
- Used by Cadence Sigrity, Synopsys and others
“Cadence Sigrity’s electromagnetic analysis tool suite offers excellent accuracy and the company’s expertise is especially valuable in tackling challenges associated with 2.5D and 3D IC designs.”

Suk Lee
TSMC, June 1, 2011
XcitePI is a full-chip power integrity solution targeting on chip / system co-design applications. It supports early chip power planning, IO and core model extraction, and simulation in both the time and frequency domains.
XcitePI
Primary Advantages

✓ Performs both transient and frequency domain analysis of on-die PDN including packaging effects
✓ Easy what-if analysis of decoupling capacitor placement, and power grid and bump design changes
✓ Generates full-chip PDN models with high pin resolution and compact circuit size
✓ Quickly checks IO power/ground and signal electrical performance to identify potential design defects
✓ Generates IO power/ground and signal interconnect models for system-level analysis of high-speed channels and buses
✓ Supports early stage studies and post-layout verification

Power net self loop inductance at each IO cell

Power net impedance

\( L = \text{power net only} / \ R = \text{power net plus on-die circuit} \)
Sigrity Analysis Tool Bundles

**Power-Aware SI**
- SIGR556 SystemSI – PBA
- SIGR301 PowerSI
- SIGR311 3D-EM
- SIGR400 SPEED2000
- SIGR021 T2B
- SIGR011 Broadband SPICE
- SIGR031 CAD Translators

**Package Extraction**
- SIGR801 XtractIM
- SIGR201 PowerDC
- SIGR311 3D-EM
- SIGR031 CAD Translators

**Serial Link SI**
- SIGR506 SystemSI – SLA
- SIGR301 PowerSI
- SIGR311 3D-EM
- SIGR021 T2B
- SIGR011 Broadband SPICE
- SIGR031 CAD Translators

**Power Integrity**
- SIGR201 PowerDC
- SIGR301 PowerSI
- SIGR311 3D-EM
- SIGR051 OptimizePI
- SIGR031 CAD Translators

**Note:** Each bundle is a single user license. Only one of the products listed in each bundle can be run at a time.
Allegro Sigrity SI – Base + Options

- Allegro Sigrity SI Base product enables constraint-driven design
  - Options for detailed analysis, compliance and assessment

Allegro Sigrity SI (Base)

- Layout floorplanning/editing, schematic-level topology exploration and TD SI simulation, constraint development/capture, analysis model library management, design translators … SI related ERCs

Power-Aware SI Option

Serial Link Analysis Option

Package Assessment and Extraction Option

Allegro Sigrity SI Base + Options availability occurred early Q1 2013
Allegro Sigrity PI – Base + Options

- Allegro Sigrity PI Base product
  - enables basic DC Analysis and decap selection/placement guidance with “in-design” access
- Power Integrity analysis option
  - Signoff and Optimization option provides detailed verification of DC and AC PDN performance and optimization of decap values and placement

Allegro Sigrity PI (Base)
Layout floorplanning/editing, analysis model library management, design translators, PI related ERCs (screening) and first order(fast) AC/DC PI analysis
Summary

- Cadence and Sigrity
  - best-in-class stand-alone solutions, even better together
  - ASI integration progressing quickly

- Sigrity PI tools bundle addresses all DC and AC PI analysis needs
  - upgrade path to ASI Base + Options

- ASI PI Base + Options solution
  - will provide the industry’s first constraint-driven PI flow
  - enables design engineers to put the right decaps into the schematic, associated with the right ICs
  - enables layout designers to address IR drop issues in-design
  - enables PI engineer to move their value-add upstream in the design process (and sign off on much higher quality PDN designs)